A NOVEL ASYMMETRIC GATE RECESS PROCESS FOR INP HEMTs

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Abstract

An asymmetric gate recess process has been developed for the fabrication of InP-based HEMTs with improved breakdown voltage. This process is based on a double e-beam exposure of a 4-layers stack of PMGI and PMMA resists. Vertical patterns can be fabricated that can otherwise not be achieved with standard e-beam lithography processes. A 30% improvement of the on-state breakdown voltage of 0.2 µm InP HEMTs was obtained without marked degradation of $f_{\text{max}}$.

I Introduction

Due to outstanding high-frequency performances, InP HEMTs are well suited for low power applications in the mm range. They, however, show limited performances when used in power amplifiers [1] because of the low on-state breakdown voltage ($BV_{\text{on}}$) that impairs large voltage swings. It is now widely accepted that impact ionization plays an important role in on-state breakdown voltage. A very promising way to alleviate impact ionization is the fabrication of HEMTs with asymmetric gate recess. This asymmetric recess increases the gate-drain spacing to distribute the voltage drop over a wider region [2-4]. We have used a new PMMA and PMGI resist combination and double e-beam exposure to achieve large gate recess asymmetry.

II Device fabrication

For this study, we have used a commercial MBE-grown HEMT structure and our in-house fabrication process. The structure was optimized for power applications (see Fig. 1) and was from bottom to top: semi-insulating InP substrate, $i$-InAlAs buffer (300 nm), Si $\delta$-doping, $i$-InAlAs lower barrier...
(10 nm), \(i\)-InGaAs channel (50 nm), \(i\)-InAlAs upper barrier (10 nm), Si \(\delta\) doped, \(i\)-InAlAs Schottky layer (15 nm), \(n^+\)-InGaAs cap layer (10 nm). The structure was fabricated using Ge/Au/Ni/Au ohmic contacts, mesa etching and electron-beam lithography (EBL) with a Raith150 system, from Raith GmbH, Germany for the 0.2 \(\mu\)m gates definition. For EBL, PMMA (polymethylmethacrylate) and PMGI (polymethylglutarimide, from MicroChem Corp.) were combined. PMMA is developed in MIBK:IPA 1:3 while PMGI is developed in a proprietary aqueous-based solvent (Developer 101). Figure 2 shows the solubility versus dose curves for PMMA and PMGI in both developers. As can be seen, a very large contrast between PMGI and PMMA is obtained.

The samples were coated with the following resist stack (from bottom to top): 130 nm PMMA 950K, 130 nm PMGI, 430 nm P(MMA/MAA), 70 nm PMMA 50K. The fabrication of the resist profile for asymmetric gate recess proceeds as follows:

- exposure of the T-gate footprint with a central, narrow dose (450 \(\mu\)C/cm\(^2\));
- MIBK:IPA 1:3 development of the PMMA 50K and P(MMA/MAA) resist layers;
- aqueous-based development of the PMGI layer (see Fig. 3);
- exposure of T-gate head and asymmetric undercut (500 \(\mu\)C/cm\(^2\) on the large recess side, 250 \(\mu\)C/cm\(^2\) on the other side);
- MIBK:IPA 1:5 development of the PMMA 950K layer and of the gate head (see Fig. 4);
- Gate recess etch in succinic acid solution (see Fig. 5);
- evaporation of 350 nm Au;

We have optimized the electron dose for the first and second exposures with our resist development simulator [5, myspace6]. With this technique, a gate recess as large as 500 nm and as small as 50 nm can be obtained on the drain and source sides, respectively.

### III Device performances

We have measured both DC and HF performances of the fabricated devices. The I–V characteristics of HEMT devices with symmetric and asymmetric gate recess are compared in Fig. 6. It can be seen that the asymmetric recess does not result in any significant loss in current drivability. The maximum transconductance \(g_{m,\text{max}}\) for both devices is near 580 mS/mm. On the other hand, impact ionization is markedly reduced due to the spread of the electric field over a 500 nm distance instead of the usually 50–60 nm. The reduction of impact ionization is illustrated by the less pronounced bell-shape in the gate current, as shown in Fig. 7.

We have measured the on-state breakdown voltage locus of the devices as illustrated in Fig. 8 with
the gate current extraction technique [7]. Our devices showing a very low gate leakage current, we have measured \( \text{BV}_{\text{on}} \) with an extracted gate current of \(-25 \mu\text{A/mm}\) to avoid unduly stressing them. It can be seen in Fig. 8 that the breakdown voltage in HEMTs with asymmetric recess improves by as much as 30%.

The S-parameters were measured on-wafer in the 350 MHz–120 GHz frequency range with an HP 8510 network analyser. The transistors cut-off frequency \( f_T \) was extracted next from the current gain \( h_{21} \) (see Fig. 9). \( f_T \) was 130 GHz and 90 GHz for devices with symmetric and asymmetric recess, respectively. We attribute this degradation to the larger effective gate length caused by the spreading of the depleted region in the channel due to the lack of electric field confinement by the highly doped cap layer on the drain side of the gate. The maximum frequency of oscillation \( f_{\text{max}} \) was also extracted for both types of devices from Mason’s unilateral gain \( U \) as shown in Fig. 10. We found values of 210 GHz and 200 GHz for symmetric and asymmetric recess, respectively. It is interesting to note that \( f_{\text{max}} \) remains almost constant when an asymmetric recess is used. \( f_{\text{max}} \) is a relevant figure of merit for the design of high-frequency amplifiers because it defined as the frequency for which the power gain reaches unity. On the other hand, \( f_T \) is associated to the transit time of electrons in the device. The high \( f_{\text{max}} \) together with the higher breakdown voltage should therefore make the asymmetric recess technology particularly well-suited for the design of power amplifiers.

IV Conclusions

We have developed a new asymmetric recess technology based on the use of PMMA and PMGI resist and a two-step electron-beam lithography process that allows the fabrication of structures with very large edge recess up to 500 nm. The fabricated devices show DC characteristics comparable to those of metric and asymmetric recess, respectively.
HEMTs with symmetric gate recess. On the other hand, the breakdown voltage is enhanced by more than 30%. The high-frequency performance does not degrade significantly. This technology is well-suited for the fabrication of mm-wave power amplifiers.

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References


