DRY SILICON ETCHING FOR MEMS

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ABSTRACT

Silicon etching is an essential process step for the fabrication of micro-electro-mechanical systems (MEMS). As we enter the on-chip integrated sensor era, the sensing elements are typically defined after circuit fabrication. This has benefits in permitting the use of a standard technology such as CMOS and also in minimising the wafer processing after fabricating the often fragile MEMS structures. Structure definition in silicon must be carried out by dry etching when profile anisotropy is required (independent of crystal orientation), particularly for high aspect ratios. Although a variety of plasma etch tools and dry etch approaches have been reported in the literature, none have been capable of meeting the majority of MEMS dry etching needs. This paper presents a novel anisotropic silicon etch process which overcomes the limitations of other techniques and is fast becoming recognised as an enabling technology for a wide range of applications in MEMS fabrication.

INTRODUCTION

The precise requirements for the dry silicon etch process will determine the equipment suitability. For example, shallow, low aspect ratio etching can typically be achieved with standard capacitively coupled RIE etch equipment, although there may be some rate and mask selectivity advantages in using high density low pressure (HDLP) systems. However when it comes to shallow high aspect ratio etching or deep etching irrespective of aspect ratio, there is an increasing tendency to opt for HDLP plasma tools. The major benefit of operating in HDLP plasma mode is the reduction in ion collision probability as the sheath thickness decreases at higher ion density and the ion mean free path increases at lower pressures[1]. Improved ion directionality results and this in turn enhances the control of anisotropy. HDLP plasmas can be generated by a variety of excitation techniques, such as ECR, MORI, Helical Resonator, ICP, etc. Of these, the inductively coupled plasma source (whether helical or planar) offers the most stable and widest operating window. Hence the present work has been carried out in the STS-ICP system operating at 13.56 MHZ (excitation and bias frequency). Details of the plasma source technology and the STS ICP have already been presented elsewhere[1]. A schematic of the STS ICP is shown in Figure 1.

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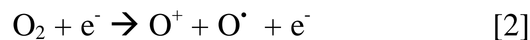
ANISOTROPIC DRY ETCHING TECHNIQUES

Simultaneous Sidewall Passivation

Several approaches can be used to inhibit lateral etching during the process and thereby maximise the anisotropy. The most successful techniques are all based on sidewall passivation and this has been suitably covered in reference 1. Simultaneous etch and sidewall passivation processes have been successfully used in CMOS and in some limited (notably shallow etch) MEMS applications. A wide range of chemistries (such as HBr, $Cl_2/SiCl_4$ or SF_6/O_2 etc.) allow suitable sidewall passivation to be formed during the etch. Here the passivation layer directly results from the chemical reaction between the dissociated precursor gas(es) and/or the silicon, possibly also with mask material contribution.

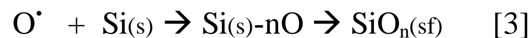
This technique can be best understood by considering a simple model of an SF_6/O_2 dry etching process. Equations [1] and [2] illustrate the formation of ion and radical species by electron (e) impact dissociation. These equations neglect S_xF_y + O interactions, which act to decrease S_xF_y polymers and increase F (radical) formation assuming the O concentration is not in saturation:

$$SF_6 + e^- \rightarrow S_xF_y^+ + S_xF_y^{\bullet} + F^{\bullet} + e^- \qquad [1]$$



$$O_2 + e^- \rightarrow O^+ + O^{\bullet} + e^- \qquad [2]$$

The role of the O is primarily seen as that of passivating the silicon surface by reacting with the silicon to adsorb on the surface to form an oxide film:



$$O^{\bullet} + Si_{(s)} \rightarrow Si_{(s)}\text{-}nO \rightarrow SiO_{n(sf)} \qquad [3]$$

where (s) and (sf) indices denote surface and surface film respectively. The surface passivation layer then must be removed by the plasma prior to etching of the Si by the F :

$$SiO_{n(sf)} + F^{\bullet} \rightarrow SiO_{n(sf)}\text{-}F \qquad [4]$$

$$SiO_{n(sf)}\text{-}nF \rightarrow^{\text{ion energy}} \rightarrow SiF_{x\,(ads)} + SiO_xF_{y\,(ads)} \qquad [5]$$

where the F adsorbs (ads) onto the surface (equation [4]) and the ion bombardment plays the

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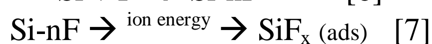
critical role in the removal of the passivation film by enhancing the adsorption, reaction and desorption. Now the F can proceed with the silicon etching by adsorption followed by product formation and desorption as a gas (g):

$$Si + F^{\bullet} \rightarrow Si\text{-}nF \quad [6]$$



$$Si\text{-}nF \rightarrow {}^{\text{ion energy}} \rightarrow SiF_{x\ (ads)} \quad [7]$$

$$SiF_{x\ (ads)} \rightarrow SiF_{x\ (g)} \quad [8]$$

Note in equation [7], when the F is saturated then the surface ion bombardment is not a critical step and the etch proceeds chemically due to the volatility of the SiF_4. However, equation [5] shows the critical role played by the ions in removing the passivating SiO_n film. Note also that the removal of the SiO_xF_y will occur as a result of either physical sputtering or by product formation of SiF_x and SO_x after ion assisted reaction with S_xF_y for example. The ion flux provides the directionality and hence controls the anisotropy of the etch. More importantly, the passivation, its removal and etching of the silicon occur simultaneously and must be in balance to maintain profile anisotropy, as shown in Figure 3. Dominance by the passivation will lead to low etch rates or even etch termination by surface residue build up. Insufficient passivation however causes a loss in anisotropy as lateral etching increases.

Plasma polymerisation reactions can be used to enhance the passivating layer, but in all cases relatively high ion bombardment energies (several hundred eV) are typically necessary to completely remove this layer from the base of the trench. In other words a strong physical component for the etch is necessary. Note, incomplete removal of this passivation component will result in the formation of grass-like residues and the appearance of "black silicon" as the inevitable rough surface results. This simultaneous sidewall passivation technique usually requires bi-level masking as photoresist masks can be inadequate in standing up to the physically aggressive nature of the process. Silicon dioxide or even metal masks are commonly used. Even so, etch selectivity to an oxide mask rarely exceeds 20:1 and etch rates range from several hundred nm/min up to 1µm/min. Chlorine and bromine based chemistries have provided some measure of success for high aspect ratios, albeit at shallow depths (<20µm) [2]. Clearly this limits the potential of this technique for MEMS applications.

Cryogenic Enhancement

In the above technique, control in passivation becomes the principle limitation as the depth increases. It is well known that the silicon-halide volatility increases with increasing halogen electronegativity. Hence F based chemistry is selected when high etch rates are required. However, precursors which liberate high levels of fluorine do result in increased etching rate, but at the expense of increased lateral etching as the sidewall passivation is

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chemically attacked by high F concentrations. One method of utilising high fluorine concentrations (whilst maintaining some degree of profile control) is to work at low substrate temperatures. Wafer temperatures in the order of -110°C have been used to reduce the etch product volatility (SiF_4 vapour pressure decreases to 100 Torr) when using a simultaneous sidewall passivation chemistry such as SF_6/O_2. This "cryogenic" temperature etching does enhance the sidewall passivation such that a few limited MEMS applications can be met where aspect ratios are <10:1 at etch depths <50μm, or where the anisotropy can be sacrificed.

The capability of a fully optimised cryogenic etch process is presented in reference 3. Here a silicon fuel atomiser was micromachined at -110°C using an SF_6/O_2 plasma. The optimised process is reported as yielding an 18μm undercut for a 275μm deep etch and an 8μm undercut for a 125μm deep etch, which corresponds to an anisotropy of A=0.94 (where $A=1-E_l/E_v$, where E_v and E_l are the vertical and lateral etch rates respectively). A micrograph of the cryogenic etch shown in the paper [3] indicates a very rough sidewall, and a smooth base with an average roughness of <0.5μm. Although such cryogenic processing clearly has some MEMS capability, it does have several drawbacks. These are mainly associated with the difficulty in using standard photoresist due to thermally induced cracking, and also some concern has been expressed in terms of surface contamination (leading to black silicon) arising from impurity condensation onto the wafer which is often the coldest surface in the chamber.

The ASE Process

Due to the inability of all of the aforementioned techniques to meet the goals for the majority of MEMS dry etch applications, STS has invested considerable resources in developing the ASE (Advanced Silicon Etch), which now provides a unique processing capability. As an illustration we begin with a direct comparison to the cryogenically etched silicon micromachined fuel atomiser application discussed above. The same devices were etched with an unoptimised ASE as shown in Figures 2a and 2b. At an etch rate of approximately 3μm/min and at 75:1 selectivity to photoresist, the anisotropy was measured to be A>0.99. Note also the micrographs show smooth sidewalls as well as the smooth base of the silicon. Average roughness has been measured at <0.15μm for the sidewall and <<0.1μm for the base. Clearly, such a capability far exceeds that available using any other technique.

As a real potential solution for dry silicon etching for MEMS, considerable attention is now being paid to this new STS ASE process. This process is based on the technique invented by Lärmer and Schilp[4], and uses a variant of the sidewall passivation technique. Rather than the sidewall protection being an integral part of the process, here the passivation is deliberately segregated by using sequentially alternating etching and deposition steps. First a sidewall passivation polymer is deposited and subsequently the polymer and silicon are etched from the base of the trench, to allow the etching to proceed directionally. In this cyclic

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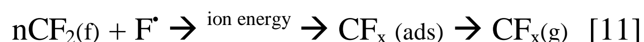
way the etching and deposition can be balanced to provide accurate control of the anisotropy.

The principle of the ASE process can be illustrated by comparing a simple reaction model with that for the SF_6/O_2 case presented in equations [1] to [8]. Consider the relatively simple deposition and etch precursors CF_4 and SF_6 respectively. Firstly the deposition precursor gas is dissociated by the plasma to form ion and radical species (equation [9]), which undergo polymerisation reactions to result in the deposition of a polymeric layer:

$$CF_4 + e^- \rightarrow CF_x^+ + CF_x^\bullet + F^\bullet + e^- \quad [9]$$

$$nCF_x^\bullet \rightarrow nCF_{2(ads)} \rightarrow nCF_{2(f)} \quad [10]$$

This passivating layer $nCF_{2(f)}$ is deposited on the surfaces of the silicon and the mask during this first step, as shown schematically in Figure 4. Here the suffice (f) is used to emphasise the deposition of the passivation film as distinct from the surface reacted film denoted by (sf) in equations 3 to 5. The gases are then switched to allow etching. During this subsequent etch step, the SF_6 firstly dissociates as in equation [1]. Next the fluorine radicals must remove the surface passivation,



$$nCF_{2(f)} + F^\bullet \rightarrow^{\text{ion energy}} \rightarrow CF_{x\,(ads)} \rightarrow CF_{x(g)} \quad [11]$$

before the silicon etching can proceed as in equations [6] to [8]. Figure 5 shows this schematically. After this, the deposition step is repeated to begin the cycle again. Here the directionality of the etch is controlled by the ion bombardment in its role of aiding the removal of the surface polymer.

Judicious chemistry selection is required to finely control this balance between the etching and the deposition. The deposited polymer must have good conformality, offer adequate sidewall passivation protection, whilst being readily removed by the etching plasma. Polymeric layers meet most of these needs[5], particularly since they need only low levels of surface ion bombardment in the presence of a reactive chemical in order to be completely removed from the surface. In this way, low self bias potentials allow the directionality of the etch to be easily controlled (which permits high selectivity to standard photoresists without compromising anisotropy). Etch precursor gases for this type of technique need to liberate high concentrations of chemical etchant to allow relatively high net processing rates taking the discrete deposition steps into account. Suitable candidates include NF_3, SF_6, etc. Polymeric deposition precursors may be based on a range of appropriate fluorocarbon chemistries such as CHF_3, C_2F_6 and higher molecular weight gases with a higher C:F ratio.

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APPLICATIONS

Based on this segregated etch and deposition step technique, STS began an aggressive development program (in late 1993) for both the equipment and the process. This has culminated in today's ASE process. The process chemistry adopted is non toxic and non corrosive and the wafer temperature is held close to the ambient, using electrostatic wafer clamping. The capability of this process on the STS-ICP system is best illustrated by considering a number of demanding MEMS applications, however the typical performance of this process is summarised in the table below and the micrographs in Figures 6 and 8.

Table I Typical results of the STS ASE process

Etch Rate	1.5 to 3.0 µm/min	Selectivity to Resist	50 to 100:1
Selectivity to SiO_2	120 to 200:1	Sidewall Profile	$90^o \pm 2^o$
Uniformity x-wafer	± 2.5 to 5.0%	Feature size	1 to >500 µm
Aspect Ratio	Up to 30	Etch Depth Capability	10 to 800 µm
These results are based on processing of 100 mm and 150 mm wafers.			

Through Wafer Via Holes

This requirement is necessary in a wide range of sensors and actuators for either making through holes for interconnects or as an element of the device itself, e.g. fluid channel etc. Competitive techniques such as wet etching (limited by its crystallographic dependency) and laser ablation (limited by high localised temperatures) have been successfully used in a number of cases. A dry etch replacement process needs high etch rates to avoid long processing times and low throughput in comparison with other steps in the serial fabrication process. The ASE process (like most other dry etch processes) has a rate/profile trade off. Figure 7 shows excellent profile control for bulk trench etching of a partially etched bore hole (350µm deep at a mean rate of 3µm/min) with an anisotropy of A=0.99. Etch rates exceeding 7µm/min have been achieved with a compromise of the anisotropy.

SOI Based Resonating Capacitance Sensors

Anisotropy is the most critical parameter to control when etching close proximity high aspect ratio structures such as sensors based on the resonating capacitance principle used in devices such as accelerometers and coriolis force detectors. After etching the beams, they need to be 'released' by removing the underlying oxide film. As the structures can be of

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relatively high aspect ratio and in close proximity, it is highly desirable to avoid wet processing not only during the feature definition but also for all subsequent processing steps. However, dry etching silicon over buried oxide has long been recognised in having problems of silicon 'notching' (or undercutting) at the oxide interface[6]. Poor profile definition caused by notching can lead to resonant frequency variations in the drive capacitance structure, resulting in degraded coriolis force detection. Furthermore, as this notching is aspect ratio dependent, the resonant frequency may further vary on the devices across the wafer causing sensor repeatability problems. The ASE process has been optimised to completely eliminate this notching effect. Figure 9 shows trenches with the critical dimension varying from 1 to 10µm (on the same wafer) etched over buried oxide. Note the complete absence of silicon undercutting at the oxide interface. This process is now being carried out in production by a number of MEMS manufacturers using the ASE process.

Membrane Based Resonating Capacitance Sensors

Resonating capacitance sensors can also be fabricated using an alternative release and isolation method such as silicon fusion bonding[7] or by engineering the sensors onto membranes. Resonating membranes (formed by back-etched cavities) have also been successfully been used for fabricating accelerometers and coriolis force detectors. Here wet chemicals are commonly used to etch cavities for membrane definition whilst dry etching is used for the critical crystal orientation independent etch steps such as defining resonating beam structures. Dry etching of wafers with back-etched cavities imposes additional processing constraints. Typically wafer temperature control relies on the use of backside helium pressurisation. This results in a pressure differential of the order of 10 Torr across the membrane. Furthermore when etching through the membrane, there is an added risk of silicon fracture rather than etching as the thickness of silicon is reduced. STS has made important advances in the equipment design as well as the ASE process to overcome these potential problems when etching membrane structures. Figure 10 shows silicon trenches etched to release structures on back-etched membrane cavities. Etch rates of 2.5µm/min were achieved using a photoresist mask and profile control was successfully maintained during the etch with A> 0.99.

CONCLUSIONS

The mechanism and capability of the ASE process has been presented. Comparing performance with other methods of dry silicon etching for MEMS applications, this is undoubtedly the most powerful, robust and flexible process, as illustrated by the range of demanding applications covered above. As a number of silicon micro-machining applications now enter into production phase using the ASE process, this technique has now been proven as the leading dry etch solution for MEMS fabrication[1, 7].

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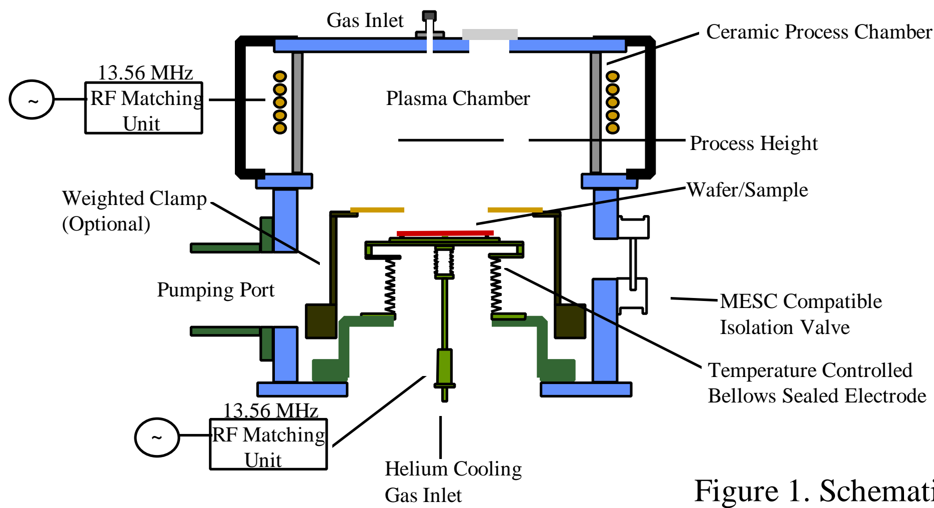
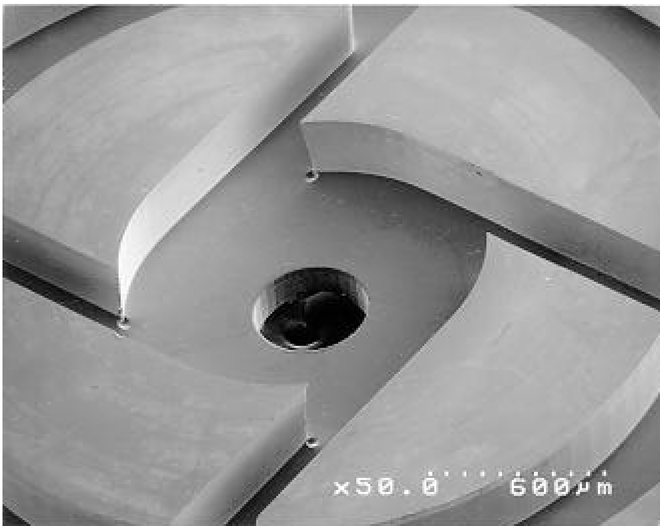


Figure 1. Schematic of STS ICP system.



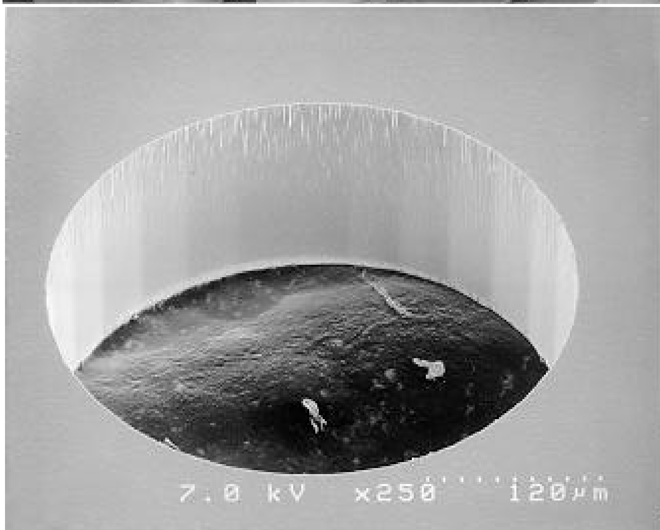


Figure 2. Micrographs of a fuel atomiser (etched using the ASE process) showing:

(a) Smooth sidewalls and base of silicon
(b) details of the “exit” hole.
Etch rate ≈ 3µm/min
Selectivity to resist = 75:1
Anisotropy > 0.99

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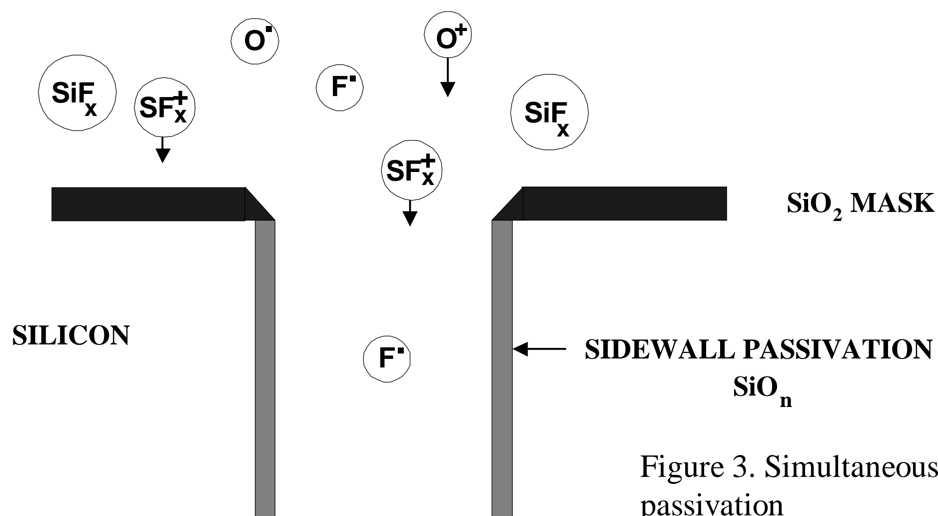

Figure 3. Simultaneous sidewall passivation

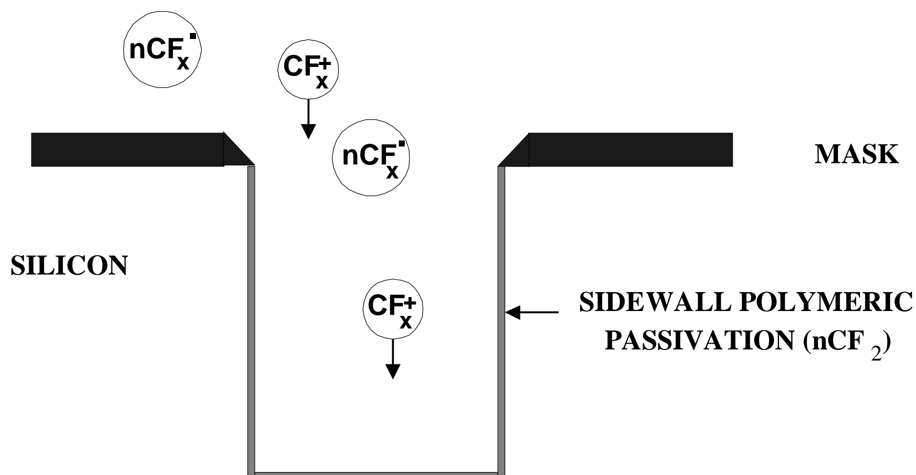

Figure 4. ASE process deposition step.

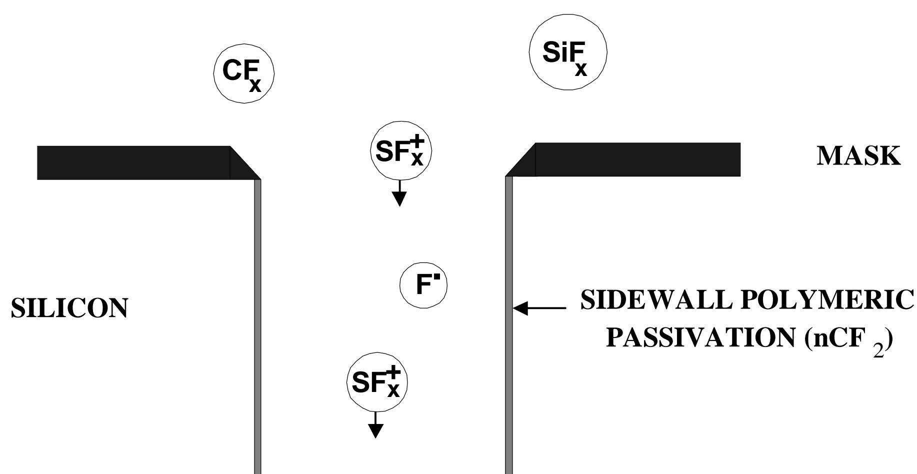

Figure 5. ASE process etch step.

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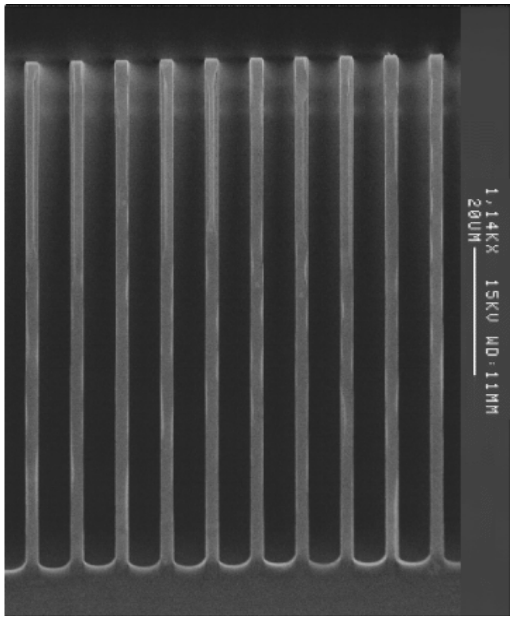

Figure 6. Micrograph of silicon trenches 80µm deep, 4.5µm space widths/2µm line widths. Aspect ratio =18, SiO_2 mask, etch rate ≈ 2.2µm/min, A > 0.99.

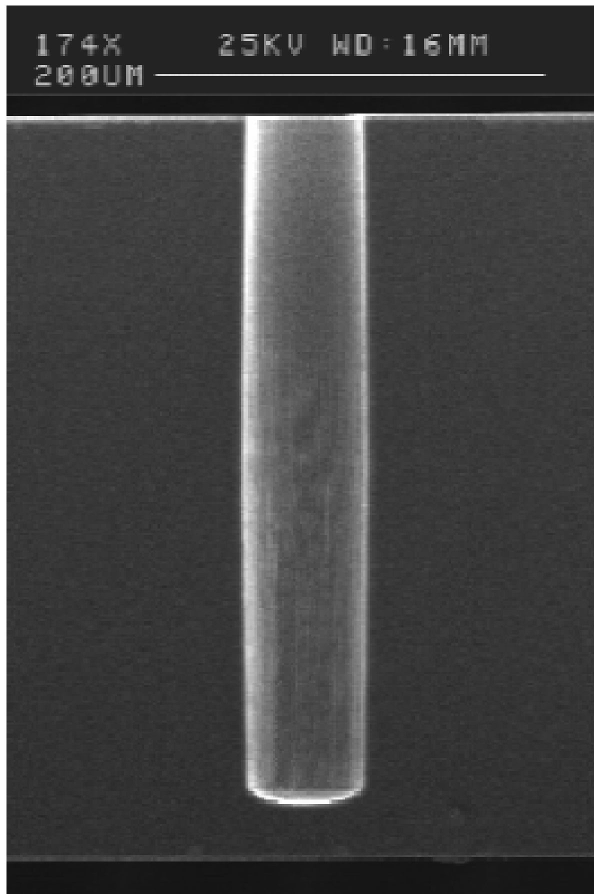

Figure 7. Cross-section of a 350µm deep bore through silicon micromachined by ASE at a rate of 2.8µm/min, A > 0.99.

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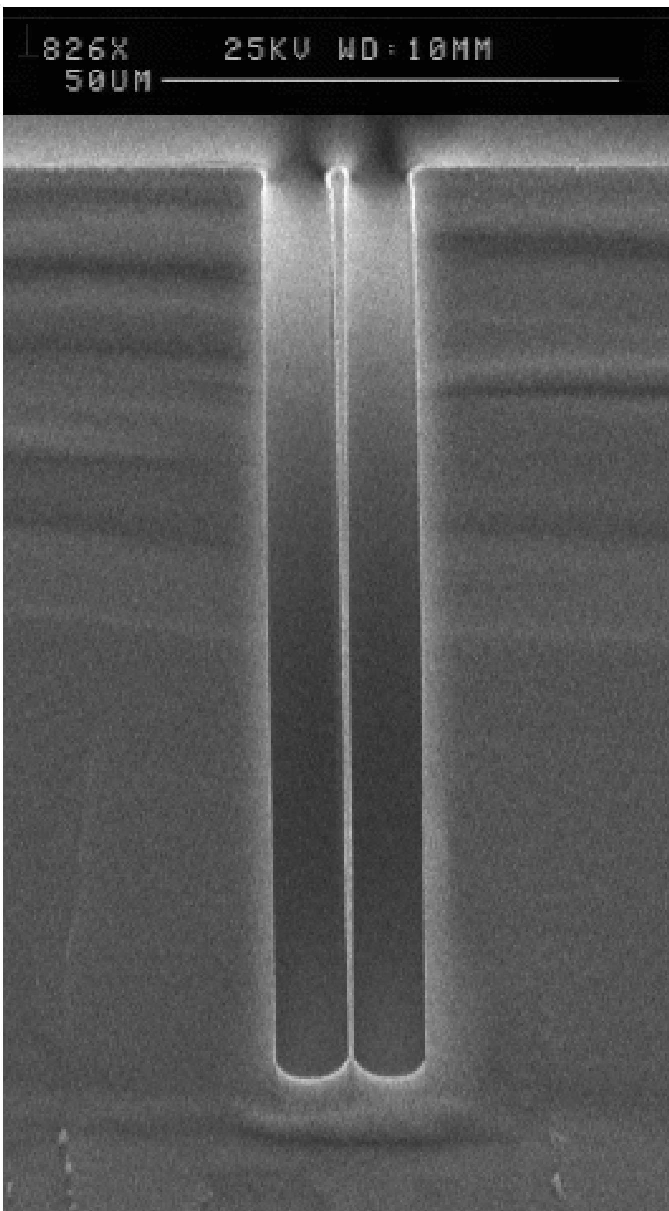

Figure 8. Silicon trench etch:
2.2 µm/min, 100 µm etch depth, 20:1 aspect ratio, 90° +/-<0.25° sidewall angle.

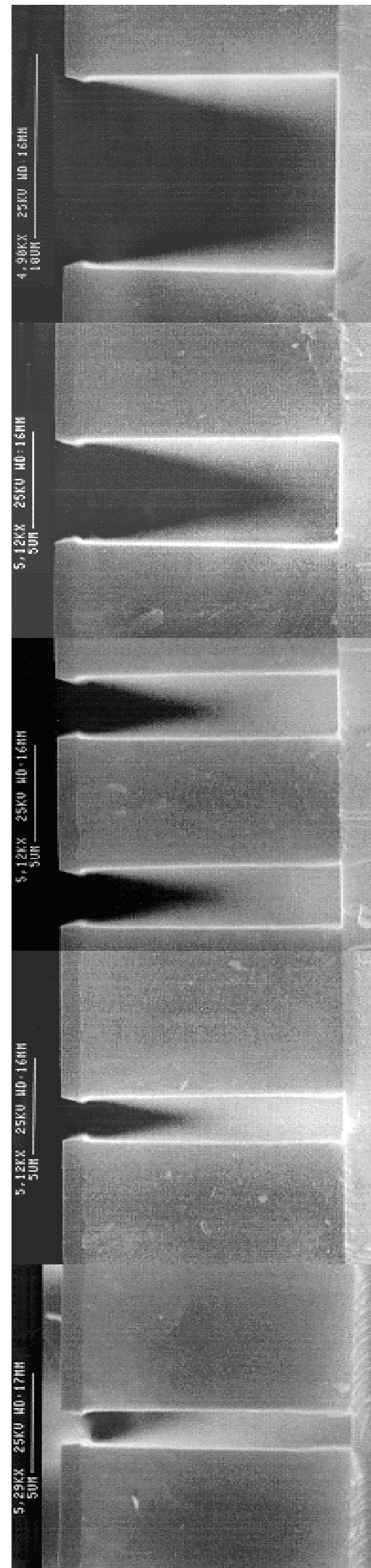

Figure 9. A series of micrographs showing 12µm deep silicon etch of 1µm to 10µm trench widths on the same wafer. Notice the absence of silicon undercutting at the oxide interface.

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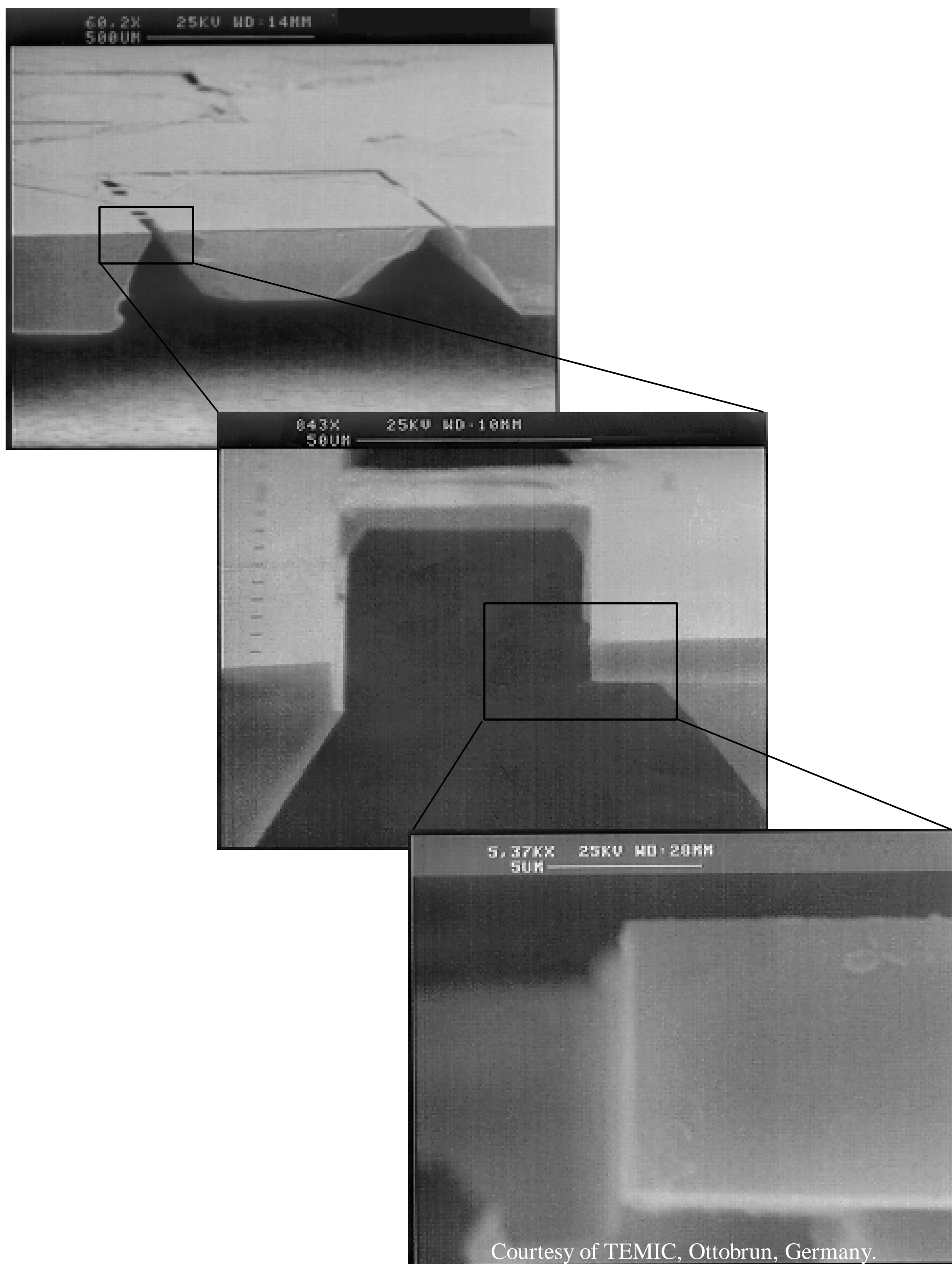

Figure 10. Micrographs of ASE process used to release a membrane structure defined by a back etched cavity. Etch rate ≈ 2.5 μm/min with A>0.99.

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