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Recent Developments, Issues and Challenges for Lithography in ULSI Fabrication

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Abstract- Nanofabrication is the core task performed and constantly further developed by today's and future semiconductor industry. Optimization of throughput and minimizing process cost and complexity thus increasing fabrication reliability constitute the main challenges within this development. As integrated circuits continue to go smaller, laying down circuit patterns on semiconductor material becomes more expensive and new techniques are required. CMOS performance has always been strictly depending on the capabilities of lithography in terms of minimum feature size and overlay. Lithography has the strongest influence on production costs of integrated circuits. In this paper, some of the recent advances in lithography are summarized with special reference to the microelectronics and nano electronics industry. Stringent demands will be made on reliability, contamination control, particle detection, and yield enhancement.

Keywords: ULSI, Electron beam lithography, nano- imprint lithography; Extreme ultra-violet lithography

I. Introduction

The purpose of this paper is to provide an overview of the motivation for the generation of lithography, important developments, issues and challenges associated with lithography. According to Moore's law of doubling functionality on a chip every two year [1] as the feature size on an integrated circuit decreases, fabricating the chips becomes increasingly difficult due to high cost and complexity of fabrication process. The fabrication of ultra large scale integrated (ULSI) devices requires the development of new technologies for deep submicron processes. As the semiconductor industry and IC industry developing quickly, there are large demands to search a method that can provide production with high accuracy and precision and good quality with low-cost and high-throughput and reliability under a fault-free environment. Among them, Micro- or Nanostructure fabrication or high-precision nano scale lithography process is the key technology to the manufacturing of photonic components, micro- and nano fluidic chips, chip-based sensors and most biological applications [2].

Some important issues like cost, complexity, reliability and in addition to these, other fundamental limits must be addressed when scaling to such small dimensions. The number of electrons in the active region of the device decreases as the physical channel size decreases. Lithographically defined dimensions will continue to shrink as device scaling enables higher speeds and greater density of transistors. Lithography equipment, resist processes, and mask-making will change to meet the challenges. Gate oxides have to become thinner requiring changes in both growth and metrology equipment. As gate oxides become thinner, voltages must drop bringing about new material requirements. Lithography will call for highly planarized surfaces, causing higher demands on chemically-mechanically polished surfaces.

The important issues in lithography process are contamination control, particle detection and yield enhancement. These changing technologies will present new reliability challenges. This paper discusses all these trends and challenges.

Lithography and the processes associated with it are the backbone of the nanotechnology revolution. Several developments are occurring simultaneously: a drive to reduce minimum feature size leading to advances in microelectronics, the use of lithographically patterned structures to prepare devices for photonics, biotechnology and other forms of nanotechnology and finally the drive to create three-dimensional (3D) structures for the creation of new materials and devices. Thus the controlled formation of nanometer scale structures in two and three dimensions are of increasing interest in many applications.

The first integrated circuits were manufactured in about 1960 (year 1 of Moore's law) and were patterned using optical lithography. Almost immediately, electron beam lithography was pursued as a high-resolution alternative and has been ever since, but optical lithography is still the preferred technique. However, after 40 years of optical lithography for the manufacture of integrated circuits, we may finally have reached the point where the cost of further pushing optical technology is no longer economically attractive. So now many lithographic techniques are considered as candidates. These techniques range from various forms of charged-particle lithography to various forms of uncharged-particle lithography and even to simple localized mechanical contact (nano imprinting). It may be that a combination of techniques is chosen in some applications or that three-dimensional integration will keep Moore's law valid without further shrinking of devices [3].

In this review, recent advances in high resolution lithography with special reference to the microelectronics industry are covered, concentrating on currant ''hot'' topics, including 193nm immersion lithography, extreme ultraviolet (EUV) lithography, E-beam direct write systems, three-dimensional (3D) two photon lithography and nanofabrication using block copolymers. Current advances in soft lithography are not reviewed due to the recent publication of several reviews in this area [4], [5]. However, step-and-flash imprint lithography is included as this technique is the method of ''unconventional'' lithography with prospects of adoption by the industry

The rest of the paper is organized as follows. Section II, presents the basic lithographic process and various types of recent lithographic techniques having numerous applications in the field of microelectronics and nanoelectronics. progress and challenges in high resolution lithographic techniques. Finally, concluding remarks are offered in Section III.

II. Overview of Lithography Process

Photolithography is a key operation in production of microelectronic as well as nanoelectronic devices. The word "lithography" refers here to a micro fabrication technique used to make integrated circuits and micro electromechanical systems (MEMS) and nano electromechanical systems (NEMS). Lithography is a highly specialized process used to transfer the patterns from mask to layer. Before the resist is applied to the substrate, the surface is cleaned to remove any traces of contamination from the surface of the wafer such as dust, organic, ionic and metallic compounds and a thin layer of Silicon dioxide is formed by a wet or dry oxidation process. The cleaned wafer is subject to priming, to aid the adhesion of the resist to the surface of the substrate material [6-7]. Lithography is a very important aspect of integrated circuit manufacturing which is very helpful in order to determine the device dimensions, which have a direct coincidence with device quality as well as cost and at last reliability also.

The important parts of a basic lithographic process are photo resist coating, exposure, development and pattern transfer. Photoresist is basically a light sensitive material used to form thin film and they may be positive and negative on the behalf of that either is more acidic or less acidic.

A. Optical Lithography:

Optical lithography is the technique for printing ultra-small patterns on to silicon wafers to make the complex circuits. It is a very important aspect of classical optical design as well as fabrication technology. It is a powerful method for patterning large areas with high throughput. Resolution is a key parameter for optical lithography which can be easily determined by wavelength of the imaging light and numerical aperture of the projection lens. Resolution can be improved by decreasing depth of focus (DOF). According the Rayleigh criterion, the DOF for small features should decrease as the feature size squared. Overcoming the DOF limits is even more challenging. Optical lithography is unsurpassed in the cost per pixel (one square unit of minimum resolution) when printing micro-sized and submicron features on silicon wafers. A lithographic process capable of manufacturing state of the art chips faces many difficult challenges. Not only must the process resolve the minimum feature size but overlay errors must be held to tight tolerances, exquisitely complex patterns must be printed with high yield, and the overall cost of the process must be acceptable. Achieving acceptable chip cost using an expensive exposure tool is strongly linked to high throughput and sensitivity as well [8].

193nm lithography has a large number of quanta within each pixel and stastical fluctuations are expected to be small. Many 193 nm quanta are used to form the image, so shot noise effects are relatively low. The high throughput levels are a key aspect to the overall cost effectiveness of 193 nm technology. Optical lithography at ultraviolet (UV) wavelengths is the standard process for patterning 90-nm state-of-the-art devices in the semiconductor industry. With such high resolution, the inherent high throughput of optical lithography will enable the development of a broad range of applications beyond semiconductor electronics. The common thread is the use of short wavelengths, 193 nm or 157

nm, coupled with immersion to further reduce the effective wavelength. As UV optical lithography has developed to enable sub-100-nm resolution, it has various applications in areas of nanotechnology beyond microelectronics applications such as nano photonics, MEMS, NEMS, nanobiology or molecular scale directed self-assembly.the transition to 193 nm projection lithography has enabled mass production of microelectronic circuits with sub-100-nmcritical dimensions. [9]

Recently , the fabrication of SET (Single electron transistor) based on top down approach, was done using optical lithography by Yongshun et al.[10].It was concluded that optical lithography approach is attractive compared to the commonly used electron beam lithography for the fabrication of SET's because it offers the possibility of integrating Si single-electron electronics with CMOS technology.

The potential advantages of immersion lithography have been known for more than 10 years, [11] , 193nm immersion lithography has taken over as the frontrunner technology for the 45nm node on the International Technology Roadmap for Semiconductors (ITRS), displacing 157nm technology. The key benefit is the possibility of constructing projection optics with numerical apertures (NAs)>1 by introducing an immersion fluid with a refractive index>1.

As promising as immersion lithography is, there are several key problems which must be addressed before the technology gains widespread acceptance, most of which relate to the use of an immersion fluid. Issues include formation of micro- or nano-size bubbles which scatter the incoming radiation and affect the imaging process, contamination of the immersion media by the resist, damage to optical components from contaminated immersion media, as well as fluid heating changing the refractive index of the media during exposure [12, [13]. One possible solution to these issues is the use of top barrier coatings [14].

B. EUV Lithography:

EUV lithography, in contrast to the classical transmission based optical i-line or DUV lithography, is running in reflection EUV offers the prospect of operating at significantly higher k and as consequence, much simpler design rules and potentially simpler OPC.laser produced plasma (LPP) and discharged produced plasma (DPP) are two main approaches used for EUV sources.EUV uses both reflective masks and mirrors for focusing and has still to surpass 193-nm-based lithography in terms of overall performance.

NA has increased from about 0.3 to 1.35 today with improvements in lens design and the use of immersion lithography. Simultaneously, the illumination wavelength has been reduced from 436 nm about 20 years ago to 193 nm for state-of –the-art scanners today explained by sivakumar et al. [15] in 2011.the 22 nm technology node, targeted for HVM in 2011, represents the last instance of using standard 1.35 NA immersion lithography based patterning for the critical layers with a k hovering right around the 0.3 value that is considered acceptable for manufacturability. According to sivakumar, the first development-quality EUV scanners are targeted to ship to end users in 2011, while the HVM versions with high targeted run rates and low targeted COO are slated for delivery beginning in mid-2012.

Recently, Wang et al. [16] present Bragg gratings in SOI strip waveguides fabricated by a single DUV (Deep ultra-violet) lithography step. Two structures were designed, one with sidewall- corrugations (named as structure A), and the other with an additional sidewall-corrugated waveguide parallel to the core waveguide (named as structure B). The fabrication of SOI Bragg gratings based on DUV Lithography was reported in [17]

C. Electron Beam Lithography:

Increasing cost and difficulty of masks make the mask based optical lithography, such as ArF immersion lithography and extreme UV lithography (EUVL), unaffordable when going beyond the 32 nm half pitch (HP) node [18]. Basically EBL lithography plays a complementary role for the optical lithography. E-beam lithography offers high resolution as compared to optical lithography due to smaller wavelength of the order of 10-50 keV electrons. Because of its very short wavelength and reasonable energy density characteristics, e-beam lithography has the ability to fabricate patterns having nm feature sizes. In EBL, a finely focused electron beam is scanned over the substrate coated with a special electron beam sensitive material called the resist (may be PMMA). Here electrons are emitted from the electron gun of a scanning electron microscope (SEM). Electron beam direct writing (EBDW) is also called as maskless lithography (ML2).The primary advantage of EBL is one of the ways to beat the diffraction limit of light and having versatile pattern formation, all such characteristics make it important for the nm regimes.

EBL is an attractive technique for fabricating nanostructures. It is suitable for nanometer scale fabrication. Recently, a large scale nanorod are fabricating by employing conventional EBL. a fast and highly scalable room temperature nanomanufacturing process for fabricating metallic nanorods from nanoparticles for applications such as interconnects and sensors was presented by Cihan et al. [19]. Metallic nanoparticles were precisely assembled in to prefabricated vias by applying a controlled dynamic electric field between the electrodes at the bottom of the vias and a center electrode placed far away from the vias. The whole of process was environment friendly and can be used to make nanorods using different types of metallic particles.the fabricated nanorods can be used for various nanoscale applications including electronic [20], photonic, and biomedical devices [21].another applications for the produced 3-D nanorods array include CMOS Interconnects [22] and plasmonic-material-based sensors [23].

Recently in 2011, Gonzalez et al. [24] suggested the use of EBL for localized micro beam irradiations. Localized irradiation of a unique device or a given sub-circuit can be conducted automatically with electron beam lithography. It is the first time that an automated procedure using this technique is use to allow performing localized irradiations of bipolar transistors. The EBL capability of the SEM used in this work enables localized irradiation of a micro circuit in order to compare and analyze the behaviors obtained for different irradiation locations.

Maskless lithography provides an ultimate resolution without jeopardy from masks, but the extremely low productivity of the traditional single beam systems made it very laborious for mass manufacturing after over three decades of development. The main limitations are of throughput i.e the very long time it takes to expose an entire silicon wafer. Since it is vacuum based technology, and bright sources do not exist, hence it results in very limited throughput. [25-28]

Several groups [29][30][31][32] have proposed different multiple electron beam maskless lithography (MEBML2) approaches, by multiplying either Gaussian beams, variable shapes beams or by using cell projections, to increase to increase the throughput. Recently in 2011, Jack et al. [33] suggested the MAPPER writing approach, the circuit layout in GDSII or OASIS format at sub-nm addressing grid, whose file size can be up to hundreds of Giga-Bytes after EPC, has to be pre-rasterized to a bit map writing format of 3.5-nm grid.

As it is a slow process, not used in high production, but utilized for low level production of semiconductor components and also used for research and development, used for photomask production, microelectronics manufacturing, used for manufacturing integrated circuits.

D. X-Ray Lithography:

X-ray lithography is the alternative process of electron beam lithography, allowing to get sub micrometer sizes of elements of charts with considerably less expenses. A perspective x-ray radiator in technology of MEMS for forming of 3D- elements is synchrotron [34, 35, 36]. X-Ray lithography has a choice of a large range of wavelengths, from about 0.4 to 100 nm. Synchrotron radiation, X-Ray is the most promising light source for transcribing super-fine patterns of less than 0.2 μm. This capability is required for 64 Mb DRAM's chips. It is not possible for conventional photolithography using ultra-violet to achieve to get such a high resolution due to spatial limitations because of optical diffractions by the mask.IBM is a world leader in the area of X-Ray lithography, where the exposure wavelength is reduced to roughly 1 nm, and a two hundred-fold reduction from deep UV X-Ray lithography is expensive to perform because of the expense of operating a synchrotron [26, 27, 28, 37]

E. Dip Pen Lithography:

DPN is a direct write method based on AFM (Atomic force microscope), is also a type of soft lithography. It is a type of scanning probe lithography that uses an AFM tip of a high resolution to write on a surface. DPN is named so, after the old-fashioned dip pen (also called as quill pen) that was used in schools in 19th century. In Dip Pen Nanolithography (DPN), arbitrary nanoscale chemical patterns can be created by the diffusion of chemicals from the tip of an atomic force microscope (AFM) probe to a surface. Dip-pen lithography is one of the well known nano-fabrication tools. It has been demonstrated to pattern soft and hard materials on various substrates for example metals, semiconductors, and insulators [38- 40]. Here an AFM tip is used as a pen to transport ink materials onto a substrate, which makes it possible to fabricate small features from sub 100 nm to over a micrometer in size. AFM tip based small feature fabrication is the strength of the DPN technique in comparison with other fabrication tools, such as: micro array, micro stamping, and photolithography.

DPN has many unique characteristics that differentiate it from other scanning probe lithographic processes. DPN is a single step process which does not require the use of resist. Another important feature of DPN is its ability to

achieve precise alignment of multiple patterns. Compared with nano grafting [41], DPN does not require a preexisting monolayer and can be used when the deposited chemical must remain unconfined on the surface, such as in diffusion studies [42-44]. DPN is a single step process which does not require the use of resist. Another important feature of DPN is its ability to achieve precise alignment of multiple patterns.

Recently, a way of mass production of nano features using parallel tip-arrays has been developed [45, 46]. .Multi-ink DPN has been studied to understand a patterning mechanism and to improve resolution of multi-ink patterning [47-49]. Multi-ink DPN methodology can be used in highly integrated protein patterning, and can provide the template for the protein sensing and cell binding studies [50].The technique has been used to pattern thiol and silane modified chemicals, metals, sol-gel precursors, conductive polymers, magnetic nanostructures, and biological macromolecules such as DNA and protein.

F. Two-Photon 3D Lithography

Conventional optical lithography is often used for microfabrication. However, single-photon absorption as used in standard photolithographic techniques is limited to be a 2D process. The 3D structures required for more complex devices are currently built up by consecutive lithographic steps. Technological advances in areas such as micro- and nano-electromechanical systems [51] (MEMS, NEMS), micro fluidic devices [52] photonic crystals, [53] 3D optical data storage [54-55] require the development of fully 3D structuring capabilities at the nanometer scale. Two-photon lithography is an intrinsic 3D lithography which has the highest potential for constructing arbitrarily shaped 3D devices in a one-step process. By tightly focusing a femto second near-IR laser beam into the resin, subsequent photo-induced reactions such as polymerization occur only in the vicinity of the focal point, allowing the fabrication of a 3D structure by directly writing 3D patterns by focus or sample scanning. Two-photon lithography not only allows the fabrication of structures that are difficult to access by conventional single-photon processes, but also achieves greater spatial resolution than other 3D micro fabrication techniques by far. [56-57]

The most commonly applied two-photon technique is two photon polymerization. This is analogous to a negative tone lithographic process in that, liquid starting materials are converted into solid structures upon exposure. The desired 3D structure is fabricated via two-photon absorption and subsequent photo polymerization, followed by removal of the unreacted liquid resin. Photoinitiators and photo sensitizers are generally used to improve the efficiency of the polymerization. With this method, various micro-devices [58-59] and photonic crystals [60-62] have been readily produced with near diffraction- limit 3D spatial resolutions. More recently, a chemically amplified positive-tone two-photon system using a two-photon photo acid generator which enabled the fabrication of buried 3D structures has been reported. [63-64]

The ability to selectively remove material in exposed regions allows for efficient creation of small hollow features within a larger solid body. Such positive-tone material systems provide unique abilities in patterning complex 3D structures, such as waveguides, photonic lattices, and microfluidic structures. Although two-photon lithography provides a unique ability to fabricate a very broad class of 3D micro- and nano-objects, one limiting factor is the low throughput due to the sequential nature of the laser scanning process. A possible solution is to use dynamic diffractive optics to generate and scan a distribution of independent focal points, [65] thereby resulting in a parallel rather than a serial process. Due to its versatile nature, it is generally believed that two-photon lithography could become a useful and powerful technique in future micro- and nanotechnology.

G. Nanoimprint Lithography:

NIL is one of the most promising nanolithography techniques which have demonstrated sub-10 nm resolution and high throughput at low cost [66-69].nanoimprinting is perspective for use in different scientific directions in biology, chemistry and materialogy.it is a cheap, providing high yield and high performance technology. During the last years imprint tools have been steadily developed and improved, such as the MII's "Imprio" series, and no showstopper could be identified so far. The imprint lithography has now been included on the ITRS lithography roadmap at the 32 and 22 nm nodes. Step-and-flash imprint lithography is a unique method for printing sub-100 nm geometries [62-63]. Relative to other imprinting processes, S-FIL has the advantage that the template is transparent, thereby facilitating conventional overlay techniques. S-FIL might provide sub-100 nm feature resolution fairly inexpensively compared to optical lithography. Nanoimprint lithography (NIL) is a new technology that circumvents the low throughput limitation of EBL. It is also a best method for fabricating nanometer scale patterns. This technique uses an electron beam fabricated hard material stamp (or mold) to stamp and deform a polymers or resist. Here the resist coated substrate is stamped and finally an RIE etching is performed to remove the resist residue in the stamped area. It is

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basically a 3D-patterning process it have so many applications in fabrication of novel nanodevices and nano materials. It plays an active and vital role in the field of microelectronics, nanoelectronics, used to fabricate devices for electrical, optical, photonic and biological applications, used to fabricate nanoscale photo detectors, silicon quantum dot transistor, quantum wire, ring transistors and biosensors. Successes of nanotechnology by substantial appearance depend on development of methods of nanolithography

. Paolo Lugli et al. [70] discusses various version of NIL such as UV-NIL, room-temperature NIL (RTNIL), combined thermal and UV-nanoimprintlithography (TUV-NIL), Molecular-Beam Epitaxy MBE-RTNIL. Some other version suggested by Nevludov et al. [71] are UV curing lithography (P-NIL - photocuring NIL), Hot embossing T-NIL-Thermal nanoimprinting, Reversal imprinting, Nanocontact printing, μ-contact printing (μCP), Nanotransfer printing. The highest resolution patterning demonstrations of sub-20 nm were performed using step and flash nano imprint lithography (SFIL) by Willson [72]. UV-Nanoimprint replication process finds various applications such as micro-lens arrays, optical elements and nanoimprint lithography.

However, since imprint technology does not reduce dimensions the quartz template fabrication for the monomer printing appears presently to be the most critical part. The imprinting process exactly replicates the template feature onto the wafer. Parameters like resolution, uniformity, linearity, placement accuracy and defectivity are to a first order determined by the quartz template. Accordingly, progress and acceptance as well as possible applications of the nano imprint technology depend on the performance and availability of related templates. At present, the realization of defect free quartz templates with a complex pattern of feature sizes down to 32 nm and below appears challenging. By employing Gaussian beam pattern generators, the targeted resolution can easily be realized. The throughput, however, is not yet acceptable. In addition, present tools suffer from placement inaccuracy. In contrast, variable shaped e-beam (VSB) writers, primarily used as photo mask pattern generators, provide the required placement accuracy and throughput, but most of them cannot meet the ultimate resolution target.

240 nm patterning using photo-curable resin for electronic devices was suggested by Sakai et al. [73]. Roller-type Nanoimprint Lithography (RNIL) was proposed by S.F.Chou et al [74].Thompson et al. [75] suggested the critical dimension uniformity and process latitude for 32 nm imprint masks. Ishizuka et al. [76] utilized sub-300 nm nano imprint patterning for the fabrication of uniform gratings on composite semiconductors. Hirai et al. [77] discusses High-aspect-ratio nano imprint patterning over 20 with 80 nm. Submicron-level three dimensional structures using nanoimprint lithography were given by Kehagias et al. [78].

Recently, Kreindl et al. [79] discovered a high accuracy, high precision and cost effective mastering process for wafer level camera image sensor applications using step-and-repeat nanoimprint lithography. A metal master pin was replicated in to a soft stamp, which was used for the fabrication of large area masters in a step-and –repeat UV-nanoimprinting process.

H. Nanofabrication with Block Copolymers

Block copolymer nanofabrication can provide large-area periodic functional structures or objects with feature sizes of the order of tens of nanometers. However, in many applications, such as multifunctional on-chip bioseparations, simple periodic structure is insufficient and spatial control of the micro domains is necessary.

Besides photolithographically patterned substrates, other lithographic methods have also been used to form patterned substrates for the purpose of achieving spatial control over block copolymer nanostructures.

Although E-beam lithography can give excellent spatial control of functional micro domains, this direct-write patterning process is not time-efficient for large-area integration of functional devices. In the case of the soft lithographic approach, long processing time is an issue and the spatial control of nanostructures has been limited by the physical contact nature of the process. Techniques for rapid patterning of functional nanostructures are thus needed for real-time applications.

Ober and coworkers have successfully developed a novel block copolymer system, poly (a-methylstyreneblock- 4 hydroxystyrene) system, [80,81] to achieve spatial control through high-resolution deep UV lithographic processes. Through the incorporation of high-resolution PHS photo resist and thermo degradable poly (a-methyl styrene) in the block architecture, large-area uniform nanometer sized pores in submicron-sized patterns were generated through simple fabrication processes. Additionally, this block copolymer was automatically aligned with vertical orientations during spin coating over a wide range of film thicknesses (40nm–1mm), thereby avoiding tedious alignment procedures. Nealey and coworkers recently reported that ternary blends (consisting of PS-b-

PMMA/PS/PMMA) capable of self-assembling on chemically patterned substrates to form periodic arrays.[82] Although self-assembling building blocks for microelectronics have yet to be fully accepted by the industry, further research in this field will doubtless help stimulate development of the next generation of devices.

III. Issues & Challenges:

Lithography is a key technology in semiconductor manufacturing. It determines the device dimensions which affect not only the device quality but also its product amount and manufacturing cost. Miniaturization is a basic key concept in modern ULSI fabrication technology. Many of components used in modern products are getting smaller and smaller. with advancement in technology ,integrated circuit came in to existence with their generations as SSI(small scale integration),MSI(Medium scale integration), LSI(Large scale integration), and VLSI(Very large scale integration), and fifth one generation that is ULSI(Ultra large scale integration). Today the central themes of electronics are reliability, low power dissipation extremely low weight and volume, and low cost, coupled with an ability to cope easily with a high degree of sophistication and complexity. Reliability is nothing it's just the probability of a system (here integrated circuit and other electronic components) for a long period of time without any fault and errors.

As the feature size on an integrated circuit decreases according to Moore's law of doubling functionality on a chip every two years, fabricating the chips becomes increasingly difficult, also the cost and functionality of the fabrication process increases greatly All such parameters are related to reliability of integrated circuits.

If we talk about reliability then cleaning is the one of the most important aspect of integrated circuit fabrication technology. Any type of dust particles and contaminants may damage the whole system reliability. Reliability is nothing it's just the probability of a system (here integrated circuit and other electronic components) for a long period of time without any fault and errors. All reliability issues concerned with integrated circuit fabrication are directly and indirectly related to the clean room technology environment. Basically, clean room is a work area where the air quality, temperature and humidity are highly regulated in order to protect sensitive equipment from contaminations, native oxide growth, dust particles and other related harmful factors. Or we can say that clean room where there is a perfect cleanliness, which the stringent requirement for ULSI fabrication, especially in case of lithography.

Clean room may be conventional clean room and laminar flow type. The air in clean room is repeatedly filtered to remove dust particles and other impurities, high efficiency particulate air (HEPA'S) filters are used for this purpose. HEPA filters are a special type of filter that is utilized to trap a large quantity of small particles that are invisible by naked eye. As far as concerning with photolithography here our main concern over the various cleaning issues such as photolithography mask, phothoresist used, etchant used, and silicon wafer itself.

Main sources of defects are airborne contamination, small dust particles (invisible by naked eye), increased amount of molecular organic materials like amines and resists and resist cleaning materials. These are called as AMC (airborne molecular contamination). The detection of these contaminants and their effect on yield loss is a challenge to the industry.if we talk about nanotechnology, although fine nanowires and nanoislands can be formed by self-assembly, a significant number of the structures formed by any thermodynamically controlled fabrication process will be defective. The effects of defects can be minimized by basing much of the circuit on simple and dense crossbar-array architecture which can be made tolerant of defects. [83, 84]. The defect –tolerant architecture can be used even with conventional devices to reduce the need for cleaner environments as device features become smaller , and the principle has been demonstrated using conventional field-programmable gate array [83]

The evolution of integrated circuits is driven by the trend of increasing operating frequency and greater functionality on a single chip. This is achieved through down scaling of the feature size of the devices on the chip. Downscaling increases process variation and leakage current, and makes the devices less reliable.

The fundamental limitation in optical photolithography is the trade-off between speed and resolution [85, 86]. nonradiation patterning have their own challenges. For example, mechanical patterning such as nano-imprint or nanoprint is a form of contact lithography, facing issues of defect density, mask cost, mask damage, and wafer throughput. The throughput is a important issue in electron beam lithography, the depth of focus is an main issue in optical lithography, and investment cost is the major issue in X-ray lithography.

Lithography defined dimensions will continue to shrink as device scaling enables higher speeds and greater density of transistors. Lithography equipment, resist processes, and mask-making will change to meet the challenges.

As far as concerning with photolithography, the important issues are contamination control, particle detection, quality & cost, resolution, accuracy, reliability, critical dimension control, and yield enhancement.

IV. Conclusions

Lithography is fundamental to advancing any technology. For many applications, most notably electronic circuitry, smaller is better in terms of speed, power consumption, and cost. Many future lithographic technologies have been investigated. We still need to relax the requirements on critical dimension control and overlay accuracy in order to continue the miniaturization process. While the critical dimension in the microelectronic industry is continually going down Stringent demands should be made on contamination control, particle detection and yield enhancement. Now it's time that we have to focus towards power consumption also, power should also be taken in to account in order to provide a cost effective, efficient and reliable system, low power design should be used for that by paying special attention towards the static as well as dynamic power dissipations..

The progress in the lithographic techniques has been driven by the industrial needs. Industry goals and need are constantly shifting and some technologies fail and others advance more rapidly than expected. While there remains debate over the costs of many of these methods and the ability to manufacture in large volume, all the methods described in this review currently have some real prospects for acceptance. It is expected no doubt that industry will achieve its goals of mastering true nanoscale lithography. The author's hope that the reader finds this review special useful in understanding the current state-of-the-art in lithography.

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