

Direct Printing of Circuit Boards Using Aerosol Jet[®]

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Abstract

Printed Circuit boards (PCBs) are traditionally fabricated using subtractive technologies such as lithography and etching. Discrete passive and active components are typically attached by pick and place and then connected using wire bonding and soldering. In this paper we show that direct printing can replace many of the traditional steps and consequently allow circuits to be fabricated on novel substrates and 3D geometries. Specifically, we report on the integration of Aerosol Jet[®] with the printing of interconnects, passives and COTS attachment. The automated generation of the printed patterns (tool paths) is based on standard Eagle CAD PCB layout software. Multilayer circuits are fabricated by alternately printing metallic wires and a polymeric insulator. Passive components such as resistors and capacitors are printed from a library. The carbon-based resistors have a range of 50 Ω to 1 M Ω and the parallel plate capacitors range from 1 pF to 1 nF. Active devices can be incorporated into the circuit by attaching discrete IC chips with metallic and adhesive inks. The processing temperature is below 150°C for all the printing and curing steps. Overall, Aerosol Jet[®] is a cost effective method for directly printing circuits onto non-traditional substrates and is also desirable for prototyping and short-run manufacturing

Introduction

An additive process for creating printed circuit boards (PCBs) is desirable for prototyping, short-run manufacturing and printing on non-traditional substrates. The creation of functional circuits by digital printing of interconnects, combined with manual attachment of commercial off the shelf components (COTS) [1], printing of passive components [2], and in-situ feedback of device values to achieve target values [3] has been reported previously. Here we report the integration of these capabilities along with the automated generation of patterns (tool paths) for printing interconnects, passives and COTS attachment based on data from standard Eagle PCB layout software. [4] In particular, the geometry and printing parameters of the passives are computed automatically from their values listed in an Eagle library file. This automated procedure allows the creation of tool paths from the CAD layout in approximately ten minutes.

Techniques and Materials

Figure 1 shows a conceptual layout of the Aerosol Jet[®] printing apparatus. [5] Aerosol Jet printing differs substantially from ink jet printing in a number of ways. In Aerosol Jet, a liquid ink is atomized to create 1-5 μm droplets that are conveyed to a print head and focused to a narrow, high speed stream with a sheath gas. The droplets travel ballistically from the nozzle and impact on the substrate which is translated under CAD/CAM control to create the desired patterns. The flow of droplets is gated with a high-speed shutter. This approach has a number of advantages including:

- The ability to accommodate a wide range of inks with high solids loadings and viscosities from 1 to 1000 cP
- Non-contact, conformal printing with high stand-off distances of 2-5 mm
- The ability to print on textured, stepped and curved surfaces
- The ability to dynamically control the print rate to create low- and high-resistivity interconnects
- Single nozzle ink print rates up to 10 mg/min
- Printed feature sizes ranging from 10 μm to several millimeters.

The four inks utilized in this work are as follows:

- A silver nanoparticle ink from Cabot, Inc.
- A UV cure dielectric ink from SunChemical, Inc.
- A carbon-based resistive ink from Methode Electronics Inc.
- A thermal cure dielectric from EChem Solutions, Inc.

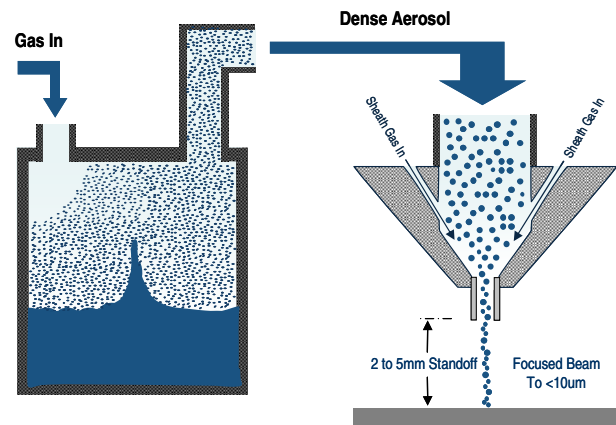


Figure 1. Schematic diagram of Optomec's aerosol-jet based printing system. Liquid inks are first atomized to create a dense, aerosol cloud of 1-5 μm sized droplets. A carrier gas transfers the aerosol to a printing head, where a co-flowing sheath gas focuses the droplets to a 10-100 μm diameter jet. The droplets impact on a computer controlled substrate to form printed features.

Interconnects

When producing a PCB, an electrical circuit schematic is first created by an engineer. The schematic is then manually translated to a physical layout like that shown in Figure 2 by the engineer or a draftsman. At this point the software can output a computer aided manufacturing (CAM) file that contains all the image information necessary for a board house to produce a PCB.

Most PCB layout software packages output the image data in a Gerber RS-274X format that contain three primitives: line *draw*, *flash* a predetermined shape, and *fill* an outline. Gerber files are designed to drive photo plotters and they employ a range of rectangular, round and specialty apertures. This work has developed a software utility for recognizing these primitives and

translating them into vector moves which are coordinated with shutter actuations. For example, an interconnect consists of a shutter open command, followed by point-to-point command to move the beam along the line and terminated by a shutter close command.

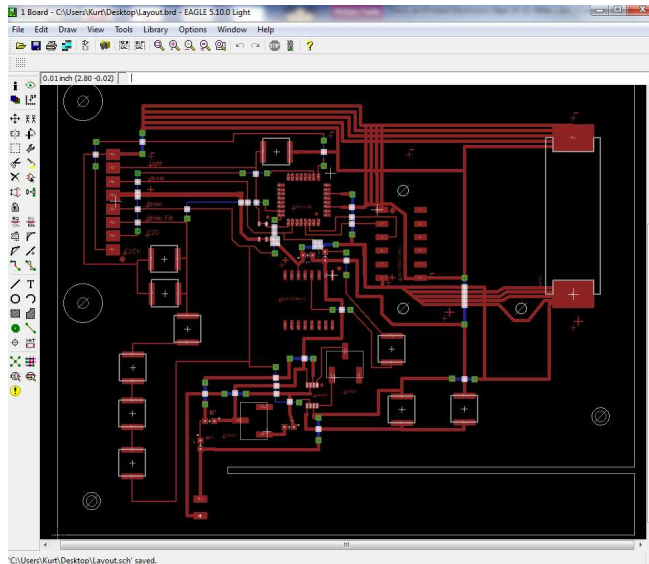


Figure 2. A circuit physical layout as seen by the designer using Eagle PCB layout software.

Complex, multilayer PCBs are typically made with multiple layers of wiring connected by vias going through the board. This 3-D structure allows lines to cross over one another without shorting. In this work, we separate the metallic layers by simply printing a layer of dielectric between the conducting lines as shown in Figure 3. The insulating pad can be localized to the region of the crossover, rather than over the entire board. Consequently, the printed, multilayer circuits can be more compact than a traditional single-sided board.

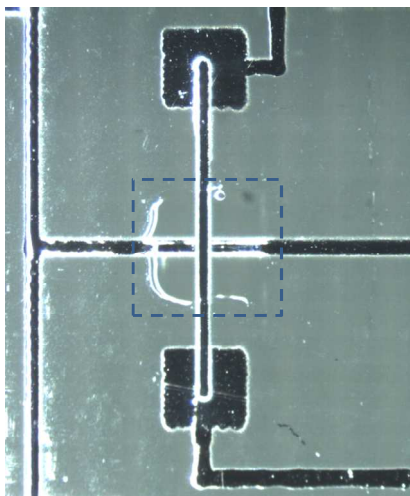


Figure 3. For multiple wiring layers, crossovers can be created by separating the metal lines with an insulating pad (inside dashed box).

The translation software recognizes the various layers files output by Eagle and uses them to form tool paths for the metal and dielectric patterns. This layer structure also forms the basis of printed capacitors. The interconnect lines can be tailored to meet specific resistance requirements. With traditional approaches, the high current capacity wires are wider than signal wires. But with the printing approach, the high current wires can be printed thicker, rather than wider. This further reduces the total layout area. On other hand, large area conductive pads and ground planes can be printed with special, large nozzle, print heads to increase the system throughput. [5]

Passive Components

Passive and active COTS that are traditionally soldered to the board are represented on layouts by the outline of their landing pads. For example, a ring of 32 pads for the 8051-class microprocessor can be seen in the layout of Figure 2. These pads are added to the layout by selecting the appropriate device from Eagle’s library. Similarly, in the new translation system, the printed passives are incorporated into the layout by selecting the specific device from the library and dropping it into the layout (Figure 4.) The printed passives also require a specified value such as resistance or capacitance value. The translation software automatically computes a toolpath to create the internal structure of the passive based on the location of the landing pads and the specified value.

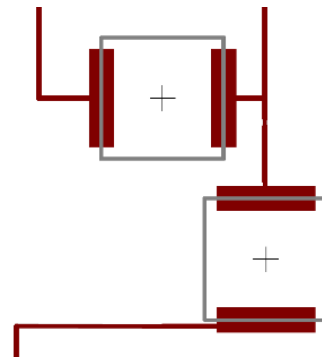


Figure 4. The circuit designer sees a typical device symbol with contact pads for connections on the circuit layout. This area corresponds to the center-left of Figure 2.

To reach the full range of specified resistance values with a single material, multiple geometries are required. For instance, thin serpentine geometries are appropriate for high values, whereas thick, wide traces are used for a medium value resistor. The translation software automatically selects the appropriate geometry based on the resistor’s value and nominal line resistance. The geometry of the serpentine resistor shown in the lower half of Figure 5 is computed using the nominal resistance of a certain line geometry, e.g. 500 Ω /cm when printed at 10 mm/sec, along with the target resistance to determine the total length. Fine tuning of the resistance value is accomplished by printing a calibration feature. Based on the value of the calibration feature, the run-time software will compensate by adjusting the print velocity.

As with the resistors, various parameters in a parallel plate capacitor, such as the area of the metal plates, the dielectric

thickness and dielectric constant will determine the capacitance value. The capacitor shown in the upper left of Figure 5 was generated by the translation software from the nominal capacitance of the device (in pF/mm²) and the target capacitance. The translation software controls both the area of the electrodes as well as the thickness of the dielectric layer. Fine tuning of the capacitance value is accomplished with small changes in the area of the top electrode. The best results are achieved by printing a calibration capacitor, and then modifying the dielectric thickness and top electrode area to achieve the target value.

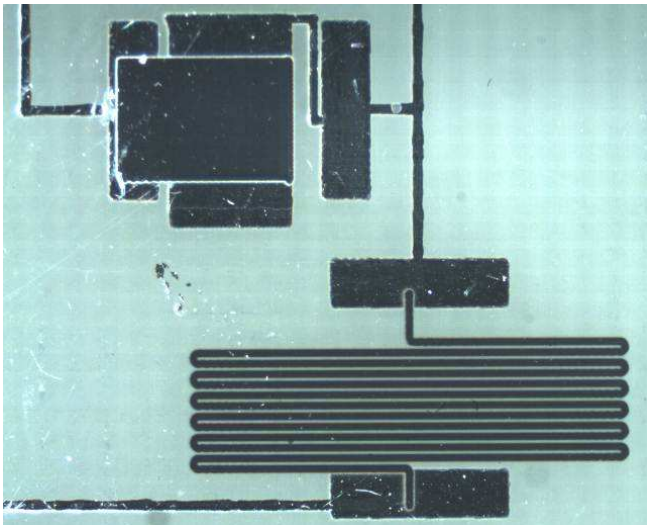


Figure 5. The geometries required to achieve the target values of resistor (LR) and capacitor (UL) structures are calculated automatically.

Although this paper only reports on resistors and capacitors, generally any component that can be printed by Aerosol Jet[®] can also be included in the EAGLE library and incorporated into a circuit. Figure 6 shows an example strain gauge and an interdigital sensor. Active devices such as carbon nanotube- and organic-transistors [6] have also been demonstrated.

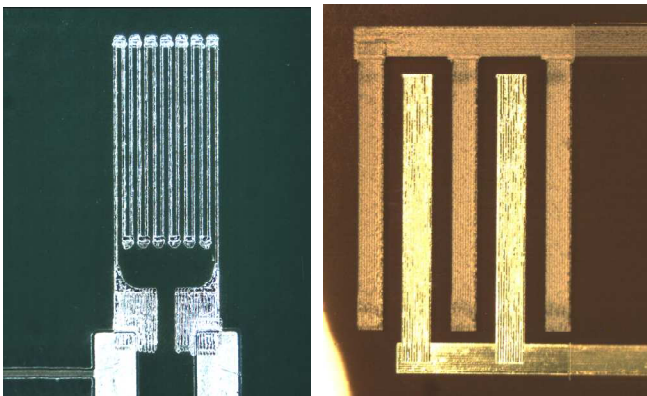


Figure 6. Future devices such as this strain gauge (L) and Cu-Ag bi-metallic sensor (R) could be included in the library.

COTS Attachment

The attachment of COTS is treated similarly to the creation of multilayer, passive components. The first layer is the landing pads which are typically printed at the same time as the interconnects. The second layer is the conductive ink that is printed over the landing pads. The COTS are manually placed on the landing pads while the ink is still wet and the parts are bonded as the ink cures. An additional layer of non-conductive adhesive can be printed after attaching the COTS. This layer provides additional adhesive strength as well as environmental protection in the bond area. Figure 7 shows a two pad (0603) device package that is attached to landing pads with a silver ink. A bonded, multiple pin device with a non-conductive overcoat is shown in Figure 8. For large COTS, a layer of strong adhesive can be placed between the COTS' body and the substrate to provide mechanical strength.

For higher throughput production, this sequence would be performed on an integrated platform containing both the Aerosol Jet[®] print head and a "pick-and-place" tool for placing the components. A slow-drying conductive adhesive would be used to allow the printing of a large number of adhesive pads before shifting to the placement tool. The high volume flow capability of the Aerosol Jet technique (up to 10 mg/min) is sufficient for supporting the adhesive pad printing at production throughputs. Further, the high stand-off distance of the Aerosol Jet print head is sufficient to overcoat and print around devices that are several millimeters tall. Larger devices would require that the print head be adjust with z-axis control.

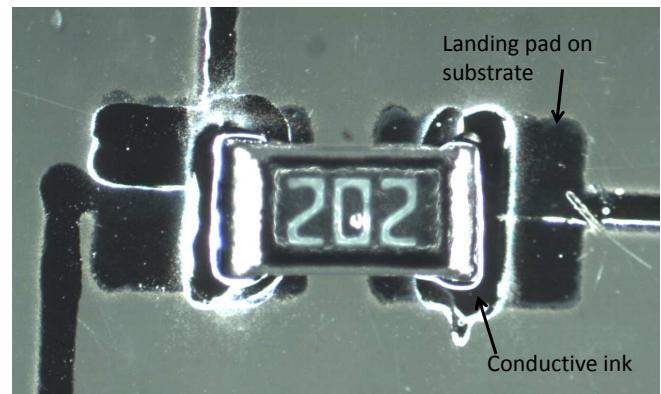


Figure 7. Small components such as this 0603 resistor (450x225 μm) can be attached.

In general, smaller COTS are easier to attach than large COTS. Large volumes of ink are required to coat and bond the larger parts. The best techniques and materials is an area of ongoing work. Fortunately, circuits are tending towards the use of smaller, not larger, COTS devices. The Aerosol Jet[®] technique can also be employed for bonding bare die. In previous work, it has been used to create 30 μm wide interconnects directly to the surfaces of bare semiconductor die. [7] Such small devices would hold benefit not just in size and weight, but also present less restriction of any flexion of the substrate or thermal mismatch between the substrate and device.

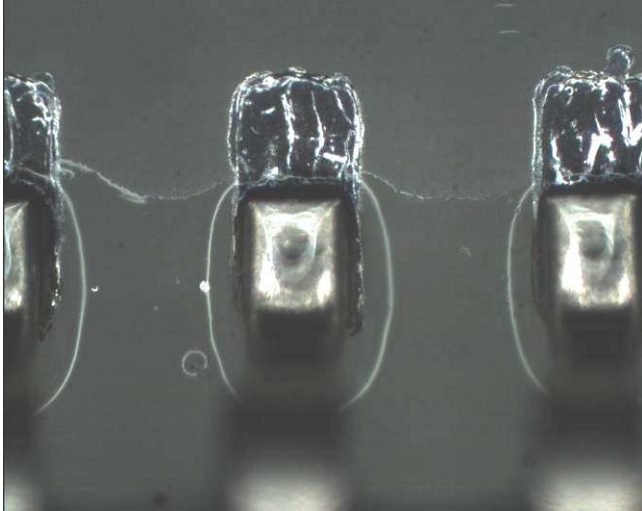


Figure 8. Silver bonds on the feet of a 0.8 mm pitch gull wing package with an adhesive overcoat for mechanical strength.

Conclusions

Figure 9 shows the completed, functional circuit board fabricated with the Aerosol Jet[®] technique from the layout in Figure 2. The tool paths were created by automated translation of Eagle's output files. Translated tool paths included those to create the printed interconnects, printed resistors, printed capacitors, and COTS attachment.

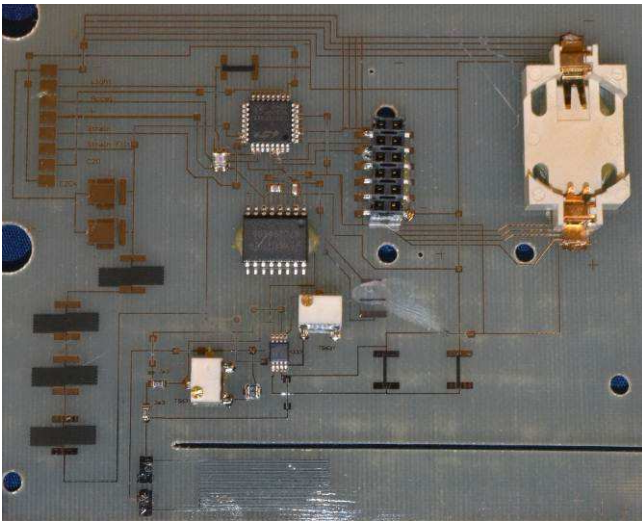


Figure9. Final circuit printed from layout in Figure 2.

References

- [1] F. Bibelriether et al., Print the Printed Circuit Board - Inkjet Printing of Electronic Devices, Proc. NIP26, pg. 715. (2010).
- [2] N. Marjanovic et al., Digital Fabrication of - Oxide Electronics, Proc. NIP26, pg. 720. (2010).
- [3] D. Mager et al., On-Line Monitoring and Feedback Control of Inkjet Printed Capacitors Using the Modular Custom Made Printing Platform Microstack3D, Proc. NIP26, pg. 726. (2010).
- [4] Eagle PCB layout software information available at: <http://www.cadsoftusa.com>
- [5] Aerosol Jet technology information available at: <http://www.optomec.com>
- [6] M. Ha et al., "Printed, Sub-3V Digital Circuits on Plastic from Aqueous Carbon Nanotube Inks," ACSNano, 4, 4388 (2010).
- [7] M. O'Reilly and J. Leal, "Jetting Your Way to Fine-Pitch 3-D Interconnects," Chip-Scale Review, 14, 18, (2010).

Author Biography

The authors work at Optomec's Applications Development Laboratory in St. Paul, Minnesota where they perform customer demonstrations of the current capabilities of the Aerosol Jet[®] process. They also participate in advanced R&D developing all aspects of Aerosol Jet printing including processes, mechanical and electrical hardware along with the required software.