High-Resolution Long-Array Thermal Ink Jet Printhead Fabricated by Anisotropic Wet Etching and Deep Si RIE

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***Abstract*—This paper describes the fabrication and characterization of a thermal ink jet (TIJ) printhead suitable for high speed and high-quality printing. The printhead has been fabricated by dicing the bonded wafer, which consists of a bubble generating heater plate and a Si channel plate. The Si channel plate consists of an ink chamber and an ink inlet formed by KOH etching, and a nozzle formed by inductively couple plasma reactive ion etching (ICP RIE). The nozzle formed by RIE has squeezed structures, which contribute to high-energy efficiency of drop ejector and, therefore, successful ejection of small ink drop. The nozzle also has a dome-like structure called channel pit, which contributes to high jetting frequency and high-energy efficiency. These two wafers are directly bonded using electrostatic bonding of full-cured polyimide to Si. The adhesive-less bonding provided an ideal shaped small nozzle orifice. Use of the same material (Si substrate) in heater plate and channel plate enables the fabrication of high precision long printhead because no displacement and delamination occur, which are caused by the difference in thermal expansion coefficient between the plates. With these technologies, we have fabricated a 1" long printhead with 832 nozzles having 800 dots per inch (dpi) resolution and a 4 pl. ink drop volume. [1085]**

***Index Terms*—Drop ejector, electrostatic bonding, micromachining, reactive ion etching, thermal ink jet.**

I. Introduction

The market of ink jet printers is growing rapidly because of its advantages, e.g., high-quality color image, low machine cost, small size, and low printing noise. There are different kinds of ink jet printers according to their actuation method. These include thermal type [1]–[5], piezoelectric type [6], acoustic wave type [7], and electrostatically driven type [8]. Among them, thermal type and piezoelectric type are the most commonly used actuation methods in commercial ink jet printers. Three important factors for ink jet printers are print speed, print quality, and machine cost. For high-speed printing, high-density nozzle and long array printhead are the important factors. The thermal ink jet (TIJ) is suitable because it is easy to array the heater (actuator) and nozzle in high density. However, the piezoelectric type needs a large actuator, therefore, a high-density nozzle array is difficult to achieve. For high-quality printing, small ink droplets that deliver high-image quality printing can be achieved using high-precision small nozzles with high ejection power. For cost reduction and smaller size, an integration of LSI into the printhead chip is the most suitable. The cost per jet in TIJ is low because the number of components is small, by which the logic circuit is easy to integrate in the head chip. Therefore, the TIJ printer fulfills these three important factors.

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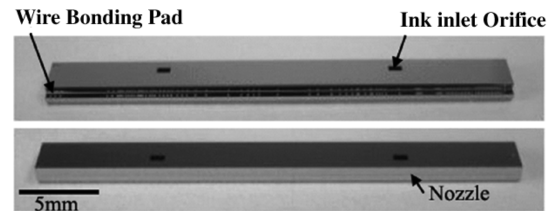

Fig. 1. Image of printhead chip.

Use of integration technologies of LSI process and Si micromachining process enable fabrication and operation of a high speed, high-image quality, and low cost TIJ printhead.

II. Fabrication Process

The printhead chip shown in Fig. 1 is fabricated by dicing the bonded wafer, which consists of a heater plate wafer, and a Si channel plate wafer. The structures of TIJ printhead chip are shown in Fig. 2, [4]. Nozzle orifice appears at the dicing plane. Because the heater plate and the channel plate are both Si crystalline substrates, there is no difference in the thermal expansion coefficient between both plates thus, chip warp does not occur. This printhead is, therefore, suitable for long chip concept. In the following sections, the primary process technologies for the printhead chip are presented.

A. Heater Plate

The heater plate consists of logic MOS LSI, embedded high voltage (HV) MOS transistor, Poly Si heating resistor and polyimide film, which protects the device from ink attack. The polyimide film is patterned by O_2 plasma RIE. The process steps are (a) The polyimide is coated and cured at temperature (350 °C) above the glass-transition temperature (285 °C) to enhance the durability against ink. (b) The polyimide film is planarized by chemical mechanical polishing (CMP). (c) The polyimide film is patterned by O_2 plasma RIE by using a mask of Si-containing resist. The polyimide used was Durimide 7520 polyimide from Arch Chemicals Inc. having a final thickness of 10 μm.

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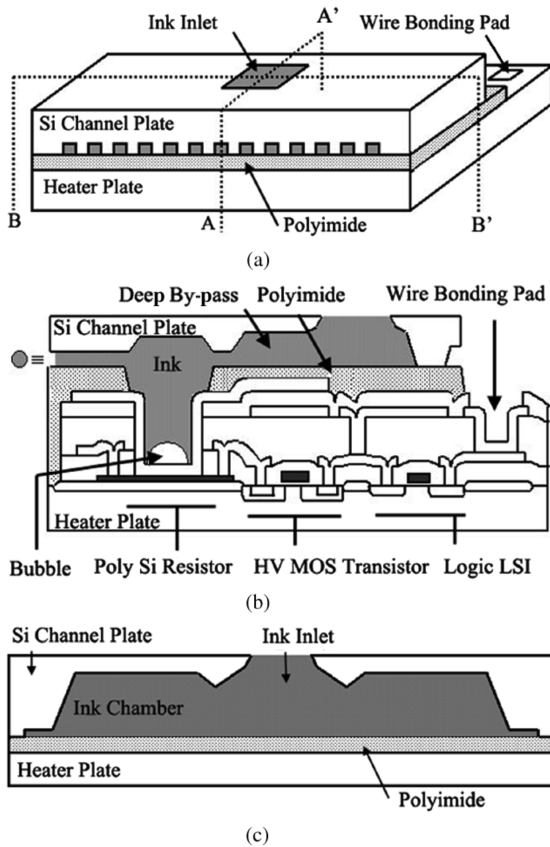

Fig. 2. Schematic diagram of TIJ printhead. (a) Perspective view of chip. (b) A−A′ cross section. (c) B−B′ cross section.

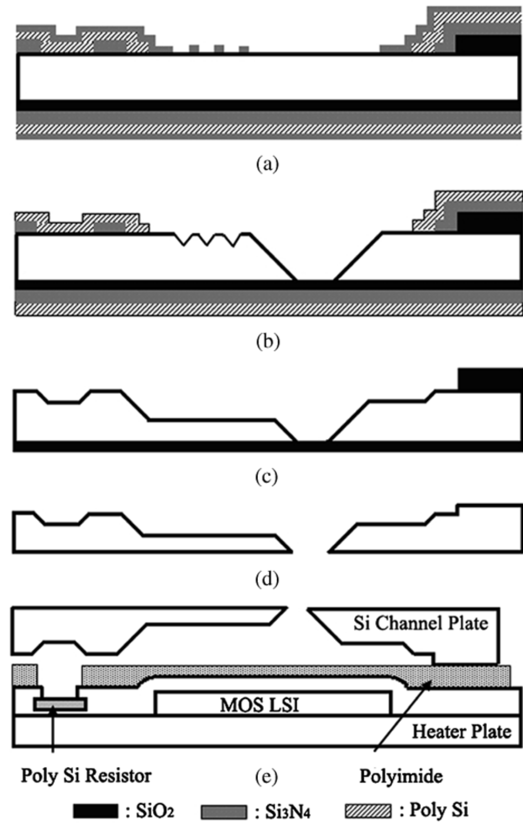

Fig. 3. Process flow of Si channel plate. The figure corresponds to B−B′ cross section of Fig. 2.

B. Si Channel Plate

Si channel plate consists of ink inlet and ink chamber formed by KOH etching and nozzles formed by ICP RIE. The ink inlet is a through-hole structure to supply ink from the ink tank to the ink chamber. The ink chamber is connected to each nozzle. The fabrication process is shown in Fig. 3. The figure corresponds to A−A′ cross section of Fig. 2(a). The process consists of 2-step KOH etching and 1-step ICP RIE. The process steps are as follows. (a) All the etching mask layers are formed by thermal SiO_2 film, LPCVD Poly Si film or LPCVD Si_3N_4 film. The process requires four mask layers. (b) The first KOH etching is performed, followed by the removal of the first Si_3N_4 film using H_3PO_4 solution. Here, the Poly Si film represented on top of the wafer serves to protect the second Si_3N_4 film from the H_3PO_4 solution. In this step, the ink inlet (through-hole structure in the Si substrate) is formed. (c) The second KOH etching is performed, followed by the removal of the second Si_3N_4 film using H_3PO_4 solution. In this step, the channel pit and the deep bypass are formed. The deep bypass is for connecting the ink chamber and channel as shown in Fig. 2(b). To form the deep bypass, the triangular sacrificial pattern represented in Fig. 3(b) is used. (d) The Si substrate is etched using an ICP RIE, followed by the removal of the SiO_2 film using HF solution. The shape of nozzle orifice is rectangular because of anisotropic etching. And the depth of the ICP RIE corresponds to the height of the nozzle orifice. In this step, the Si channel plate is completed. (e) The Si channel plate wafer is bonded to the completed heater plate wafer.

In the ICP RIE of Si, a deposition step (sidewall passivation) and etching step are performed subsequently. During the etching steps, the sidewall polymer deposited in the previous steps prevents the etching of sidewall Si due to off-vertical ion impact. On the other hand, the bottom polymer is etched off by vertical ion impact and subsequently the underlying Si substrate is etched. To achieve anisotropic etching, the balance of deposition and etching is important. This balance is greatly affected by the deposition and etching time. In the present application, there is a slope formed by the KOH etching in addition to the bottom surface and the sidewall surface. On the structure with sloped surface, the influence of RIE conditions on the etching shape is investigated. Fig. 4(a) shows the schematic diagram of sample structure before RIE. Under low deposition condition, sidewall surface is etched and exhibits an isotropic shape as shown in Fig. 4(b). On the other hand, under high deposition condition, grass is formed on sloped Si surface whereas no problems are observed on the bottom surface and the sidewall surface as shown in Fig. 4(c). The reason for the grass formation on the sloped surface is that the deposited polymer is not completely etched off by ion impact in the etching steps and acts as micromask. This is explained in Fig. 5. The sloped surface is considered to take an intermediate state between bottom surface and sidewall surface. Finally, under well-balanced conditions, the ideal topography is obtained on every surface as shown in Fig. 4(d). On extremely high deposition conditions, the grass is formed even on the flat surface [9].

Next, the structure of nozzle is discussed. Fig. 6(a) and (b) shows SEM micrographs of nozzle in the steps of Fig. 3(c) and

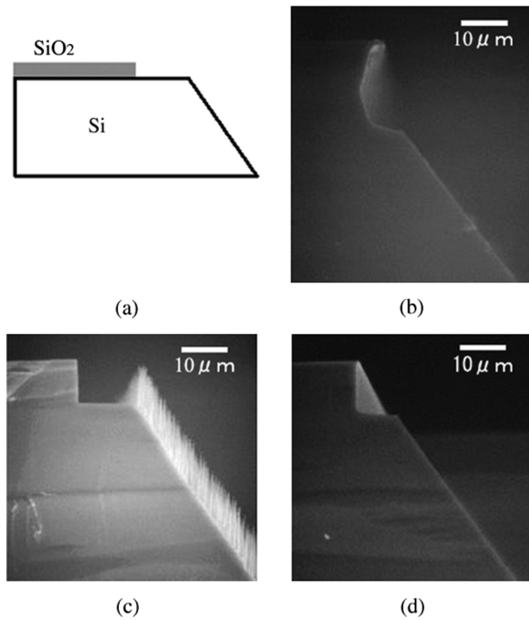

Fig. 4. Cross-sectional SEM photographs of Si channel plate formed under different RIE conditions. (a) Schematic diagram of initial sample structure (before RIE). (b) Under low deposition conditions ($\text{deposition time} = 5$ s, $\text{etching time} = 12$ s). (c) Under high deposition conditions ($\text{deposition time} = 5$ s, $\text{etching time} = 6$ s). (d) Under well-balanced conditions ($\text{deposition time} = 5$ s, $\text{etching time} = 9$ s).

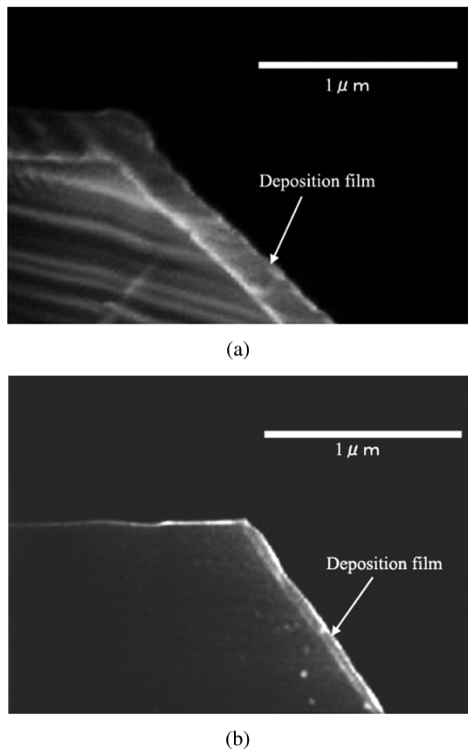

Fig. 5. Difference in thickness of deposited film between flat region and sloped one. The deposited film remains on the sloped surface. The difference explains the grass generated only on the sloped surface. (a) After deposition of passivation film. (b) After ICP RIE.

(d), respectively. Before ICP RIE of the nozzle, the channel pit is formed inside each nozzle by the second KOH etching in Fig. 3(c). The nozzle formed by ICP RIE has the squeezed structures in the front end and the rear end. The squeezed structures contribute to the high-energy efficiency of printhead, i.e., low-power consumption and high ink drop energy [5]. The low-power consumption contributes to the decrease in rise of temperature during the printing operation and therefore the suppression of air bubble defect formed in the nozzle or ink chamber. On the other hand, the high ink drop energy contributes to an enhanced ink drop velocity and therefore successful ejection of small ink drop. ICP RIE also forms the chip-in filters arranged behind the nozzles. The chip-in filters prevent the penetration of particles in the ink into the nozzle, and therefore suppress the misfire of ink drop. The squeezed structures and the chip-in filters fabricated using ICP RIE process attribute to the high flexibility and the high patterning accuracy of complex designs.

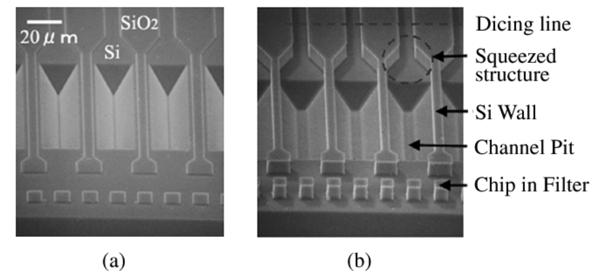

Fig. 6. SEM micrographs of nozzle. (a) Before ICP RIE. (b) After ICP RIE.

The jetting characteristics of ink jet printhead, e.g., flow rate and drop volume of ink, are described by using the equivalent circuits described in (1) and (2), which include the inertance and the resistance of ink fluid pass, especially near the heater and nozzle [5], [10]. These parameters are calculated from the geometry of ink fluid pass. For this reason, it is important to provide a wide range of channel pit area (design flexibility) and describe the accurate channel pit area.

$$K = \frac{L_r}{L_f + L_r} \tag{1}$$

where K is the inertance ratio, L_r is the heater rear inertance , and L_f is heater front inertance. The inertance of each pass L is described as

$$L = \rho \frac{l_{f,r}}{S_{f,r}} \tag{2}$$

where ρ is ink density, l and S are fluid pass length and cross-sectional area.

Next, the channel pit area is extracted. Fig. 7 shows the definition of dimensions of cross-sectional area in channel pit. The shape of channel pit is assumed to change from a triangle to a trapezoid by ICP RIE. The model is based on the model same as that of bias sputter etching [11]. The area of the channel pit after ICP RIE can be expressed as follows:

$$\mathrm{S}_1 = \left(\mathrm{Y}_1 - \frac{\mathrm{X}_1}{\tan\phi}\right)\mathrm{X}_1 \quad \text{for } \mathrm{Y}_1 \leqq \mathrm{P}_\mathrm{W} \tag{3}$$

$$\mathrm{S2} = \left(\mathrm{Y}_1 - \frac{\mathrm{X}_1}{\tan\phi}\right)\mathrm{X}_1 - \frac{1}{4}(\mathrm{Y}_1 - \mathrm{P}_\mathrm{w})^2 \tan\phi \quad \text{for} \mathrm{Y}_1 \geqq \mathrm{P}_\mathrm{W}. \tag{4}$$

The parameters $\mathrm{Y}_1, \mathrm{X}_1$, and ϕ are measured by using test structures shown in Fig. 8. Fig. 9 shows the measured parameters. By

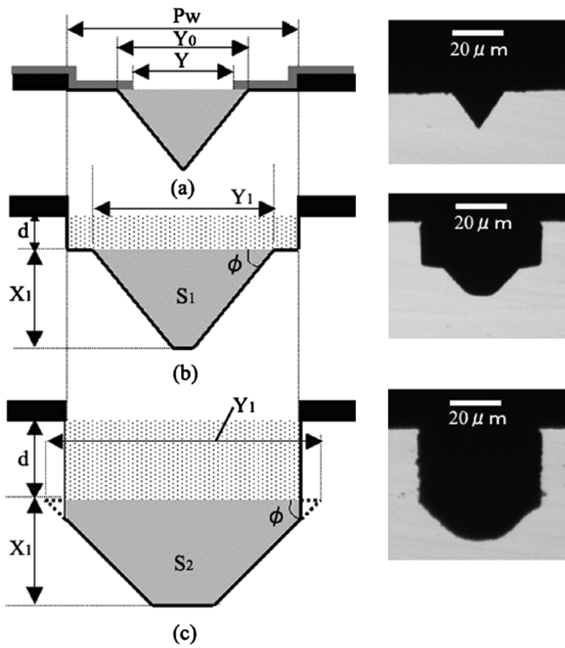

Fig. 7. Definition of dimensions of cross-sectional area in channel pit. Channel pit area is defined in the gray area. Total channel area is defined in the sum of gray and dotted areas. (a) After second KOH etching. (b) After ICP RIE $(\mathrm{Y}_1 \leqq \mathrm{P}_\mathrm{W})$. (c) After ICP RIE $(\mathrm{Y}_1 \geqq \mathrm{P}_\mathrm{W})$. (d) Depth of ICP RIE.

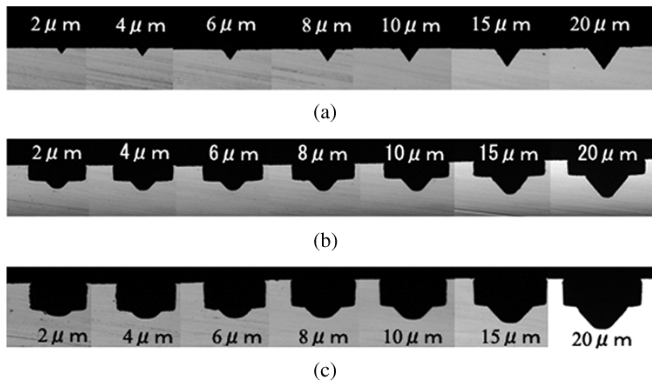

Fig. 8. Cross section of channel pit with various pit width. The length denoted on the figure is Y defined in Fig. 7. (a) Before RIE. (b) After 12 μm RIE. (c) After 20 μm RIE.

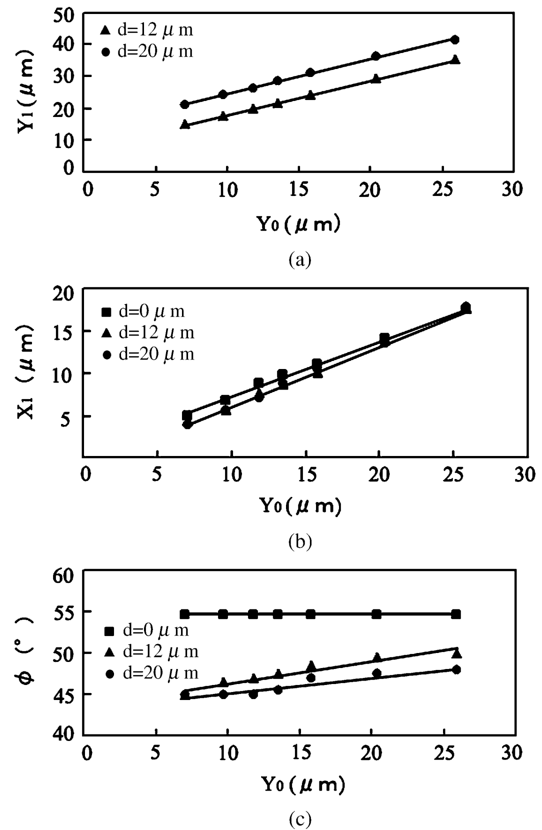

Fig. 9. Parameters measured by cross-sectional photographs in Fig. 8. Y_1. (b) X_1. (c) ϕ.

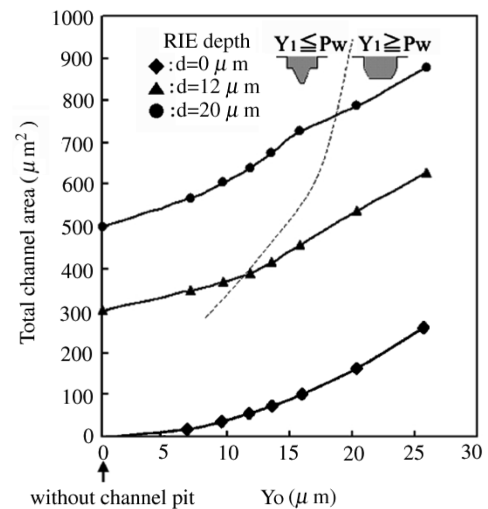

Fig. 10. Total channel area for 800 dpi nozzle. P_W is 25 μm for 800 dpi.

using these parameters, channel pit area and total channel area were calculated for 800 dpi nozzle (Fig. 10). The total channel area of the fluid pass without channel pit was 300 $\mu\mathrm{m}^2$ for RIE depth of 12 μm, while fluid pass with 25 μm channel pit (Y_0) had a total channel area of about 600 $\mu\mathrm{m}^2$. Therefore, the total channel area can be enlarged more than two times as that without channel pit.

The benefits of the channel pit are as follows:

① The jetting frequency is enhanced by decreasing the ink refill time due to the enlargement of cross section of the channel and therefore the decrease of fluidic resistance. Compared with conventional fluid pass having no channel pit, the pass resistance decreases to 86% using channel pit as described in Fig. 11. It was observed that the drop weight of conventional printhead decreases above 18 kHz as shown in Fig. 11. On the other hand, the printhead having channel pit can maintain a stable jetting at 21 kHz. Basically, thermal ink jet ejects a part of ink between nozzle and heater front end. Decrease in drop weight at high frequency means the ink refilling does not complete before the following jetting. Therefore, printhead with channel pit is effective to achieve high speed refilling.

② By heating the ink, a bubble is formed and the ink drop is ejected through the nozzle. During the dispensing, the bubble is enclosed on the heater by the channel pit, therefore preventing the expanding of bubble toward front end and rear end [12].

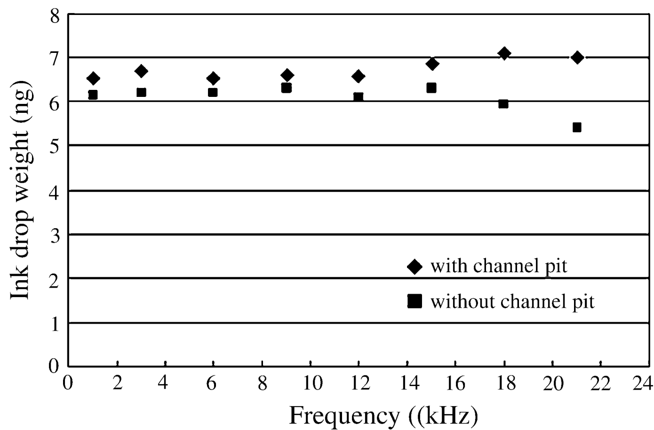

Fig. 11. Ink drop weight as a function of frequency. The total channel area of channel with pit structure was 289.1 μm^2 and the pass resistance was 119.7×10^{12} Pas/m^3. The total channel area of channel without pit structure was 221.6 μm^2 and the pass resistance was 138.4×10^{12} Pas/m^3.

③ The energy efficiency of drop ejector is enhanced by the squeezed structures in the vertical direction.

Table I shows the comparison of energy efficiency among different types of nozzles. Energy efficiency (EF) is defined as the ratio of drop kinetic energy (E_d) to the consumed energy of the heater (E_h). Conventional structure does not have squeezed structure at the front-end and rear-end. The ink used was dye based ink having a viscosity of 2.7 mPa · s, surface tension of 36 N/m and density of 1060 kg/m^3. An increase of 3.2 times in energy efficiency was observed using nozzle with squeezed structure as compared with conventional structure without squeezed structure. Furthermore, an increase of 1.4 times in energy efficiency was achieved when channel pit structure is present. Therefore, a total of 4.4 times increase in energy efficiency was achieved [5].

Next, the process flow for the ink inlet formed by through-hole and the ink chamber with Si roof is shown in Fig. 12. The process steps are same as that of Fig. 3 and are as follows. (a) The SiO_2 film remains in the region where the ink chamber is formed. (b) The SiO_2 film delays the start of Si etching on the ink chamber region as compared with the ink inlet region. The delay contributes to the etching depth difference between both regions. The ink inlet with through-hole is formed in this step. (c) The ink inlet is connected to the ink chamber in this step. The SEM micrograph is shown in Fig. 13.

The size of the ink inlet orifice is important from the view point of ICP RIE. To achieve good etching characteristics in ICP RIE process, the wafer must be controlled at appropriate temperature during the RIE. Popularly, commercial RIE equipment supplies a carrier gas, e.g., helium gas, between the wafer and the cathode electrode to control the wafer temperature. In the present application, the carrier gas is sealed from the backside SiO_2 film in the ICP RIE process as shown in Figs. 3(c) and 12(c). If the through-hole formed in Si substrate, i.e., the ink inlet orifice, is large, the backside SiO_2 membrane will be broken by the mechanical stress [13] and, therefore, the carrier gas leak to the etching chamber. As a result, the wafer temperature rises and an isotropic etching is observed. Use of small ink inlet orifice solved this problem.

C. Electrostatic Wafer Bonding

In conventional printhead, epoxy adhesive has been used for wafer bonding [14]. In this method, the excess adhesive is forced out to the nozzle.

To form an ideal shaped nozzle orifice, electrostatic bonding of full-cured polyimide to Si [15] has been applied to the wafer bonding as an adhesive-less bonding. The important factor for this bonding technique is that the full-cured polyimide is planarized by CMP. The bonding process consists of the following steps.

① The heater plate wafer and the channel plate wafer are put into contact via each front surface.
② The wafers are heated up to 350 °C on the hot plate.
③ The wafers are pressed at a pressure of 1 Kg/cm^2.
④ A voltage of 100 V is supplied between both electrodes.

Fig. 14 shows the nozzle orifice formed by the bonding method. Thus, the ideal shaped nozzle orifice is formed. And also, the bonded chip has sufficient bond strength for the present applications. Furthermore, any device damage were not observed for MOS LSI formed in heater plate in spite of the high voltage supplied during the bonding process. From these results, electrostatic bonding of full-cured polyimide to Si is highly applicable to the present TIJ printhead.

Here, comparisons are made between the polyimide bonding method and other adhesive-less bonding methods. The conventional adhesive-less wafer bonding methods are divided into two groups, i.e., the fusion bonding [16] and the electrostatic bonding of Si to glass [17]. Because the fusion bonding method requires a high temperature treatment at about 1000 °C it can not be applied for LSI wafer. And also, because the electrostatic bonding of Si to glass uses a sodium containing material (Pyrex glass), which degrades the device characteristic due to the alkali ion contamination, it cannot be applied for LSI wafer [18]. As the electrostatic bonding of polyimide to Si is performed at low temperature by using a contamination free material, thus it is applicable to LSI wafer.

D. Dicing and Surface Coating

The bonded wafer is divided into chips by dicing. The dicing blade used was a resin bond type having 2 to 4 μm diamond grit size. On the surface of dicing plane, the Si substrate and the polyimide film appears as shown in Fig. 2(a). Glass layers or other materials do not appear on the dicing plane. It is an important point to achieve a good dicing yield. This is one reason for the use of polyimide film as an adhesion layer between both plates.

Finally, the diced chip is subjected to nozzle surface coating treatment in which the fluorinated film is coated on the nozzle surface for ink repellency. As for the surface coating, Cytop is coated by soaking the nozzle surface into the Cytop solution. During the soaking process, nitrogen gas is introduced from the ink inlet orifice and is blown out from the nozzle orifice. The blowing process prevents the nozzle clogging and internal coating. After that, the film is cured in nitrogen ambient at 185° for 60 min to enhance the ink durability. Fig. 15 shows the nozzle surface subjected to this treatment. The ink repellent film

TABLE I
COMPARISON OF ENERGY EFFICIENCY AMONG DIFFERENT TYPES OF NOZZLES

	unit	Conventional structure	Squeezed structure (without channel pit)	Squeezed structure (with channel pit)
Drop kinetic energy (Ed)	nJ	0.37	1.18	1.57
Consumed energy of heater (Eh)	μJ	5.4	4.8	4.5
Energy efficiency (EF)	X 10^{-4}	0.84	2.68	3.7

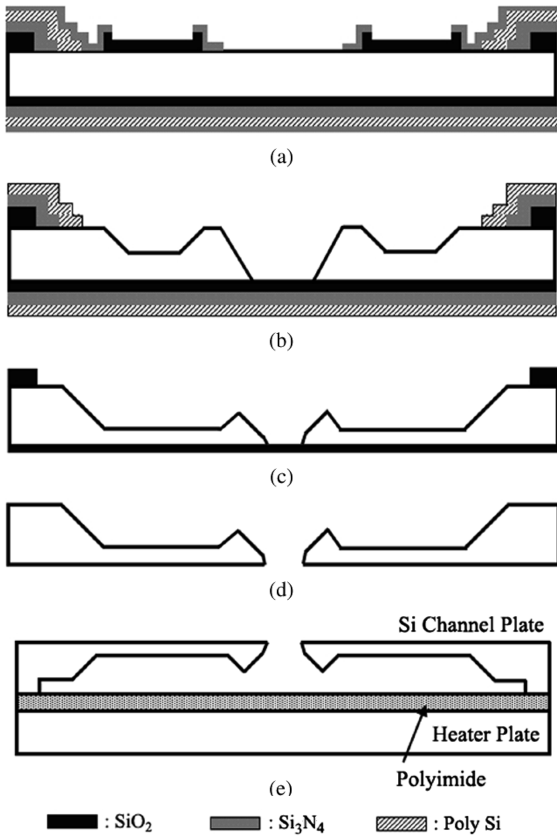

Fig. 12. Process flow of Si channel plate. The figure corresponds to B−B′ cross section of Fig. 2.

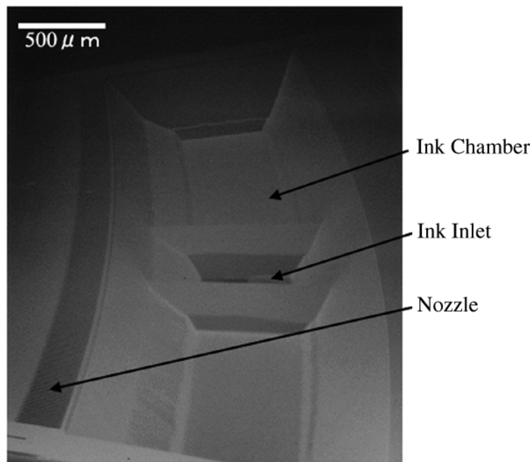

Fig. 13. SEM micrograph of Si channel plate with small ink inlet orifice.

prevents misdirectionality of jetted ink drop caused by the flood of ink around the nozzle orifice.

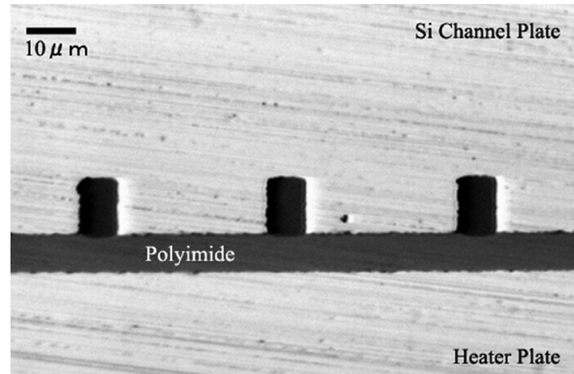

Fig. 14. Nozzle orifice formed by electrostatic bonding (800 dpi nozzle).

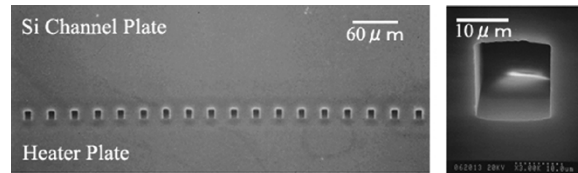

Fig. 15. Nozzle orifice subjected to nozzle surface coating.

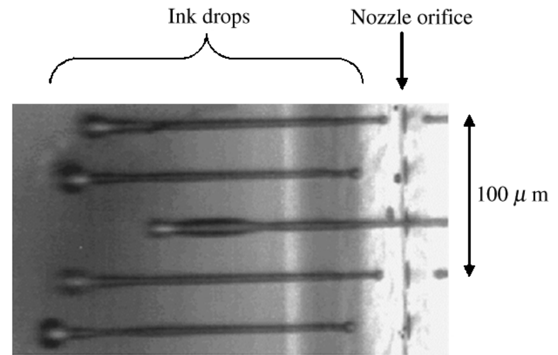

Fig. 16. Photograph of ink flight from the nozzle.

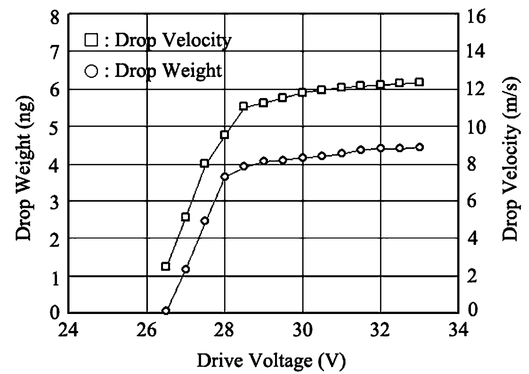

Fig. 17. Ink drop velocity and weight as a function of drive voltage.

III. Performance of Printhead

The printhead was fabricated with the above technologies. Although the printhead is long $(1'')$, delamination between both plates due to the thermal stress during the assembly process was not observed. This is because both plates are the same material (Si substrate) and therefore the warp of the chip due to the difference in thermal expansion coefficient does not occur. This enables the array of numerous nozzles (832 nozzles) and therefore enabling high-speed printing.

Furthermore, 4pl. small ink drop was successfully ejected with the sufficient ink drop velocity (12 m/s) from the 800 dpi printhead and therefore a photo quality printing was achieved. Figs. 16 and 17 shows the nozzle array jetting ink drops, and the ink drop velocity as a function of drive voltage.

IV. Conclusion

A high-resolution long array TIJ printhead has been fabricated and demonstrated to operate successfully by combining two functional Si wafers, a bubble generating heater plate fabricated using LSI process and a channel plate fabricated using Si bulk micromachining technology. Great improvement in the printing characteristics of the printhead was achieved because of the benefits from channel plate with nozzle having squeezed structure and channel pit. The nozzle formed by RIE has squeezed structures, which contribute to 3.2 times increase in energy efficiency of drop ejector and therefore successful ejection of small ink drop. The channel pit formed inside the nozzle contributes to high jetting frequency at 21 kHz and 1.4 times increase in energy efficiency. We have also confirmed high-speed printing and high-quality printing.

References

[1] P. A. Torpey and R. G. Markham, "Thermal inkjet printhead," U.S. Patent 46 638 337, Jan. 1987.

[2] I. Endo, Y. Sato, T. Nakagiri, and S. Ohno, "Bubble jet recording method and apparatus in which a heating element generates bubbles in multiple liquid flow paths to project droplets," U.S. Patent 4 740 796, Apr. 1988.

[3] W. A. Buskirk, D. E. Hackleman, S. T. Hall, P. H. Kanarek, R. N. Low, K. E. Trueba, and R. R. van del Poll, "Development of high-resolution thermal ink jet printhead," *Hewlett Packard J.*, pp. 55–60, Oct. 1988.

[4] M. Murata, M. Kataoka, R. Nayve, A. Fukugawa, Y. Ueda, T. Mihara, M. Fujii, and T. Iwamori, "High resolution long array thermal ink jet printhead with on-chip LSI heater plate and micromachined Si channel plate," *IEICE Trans. Electronics*, vol. E-84-C, no. 12, pp. 1792–1800, Dec. 2001.

[5] M. Fujii, T. Hamazaki, and K. Ikeda, "New thermal ink jet printhead with improved energy efficiency using silicon reactive ion etching," *J. Imaging Sci. Technol.*, vol. 43, no. 4, pp. 332–338, July/Aug. 1999.

[6] S. Sakai, A. Kobayashi, T. Naka, S. Yonekubo, T. Mitsuzawa, and S. Shinada, "Inkjet Recording Head," European Patent 0573 055A2, Apr. 1993.

[7] X. Zhu, E. Tran, W. Wang, E. S. Kim, and S. Y. Lee, "Micromachined acoustic-wave liquid ejector," in *Tech. Dig. Solid-State Sensor and Actuator Workshop*, Hilton Head Island, SC, June 1996, pp. 280–282.

[8] S. Kamisuki, T. Hagata, C. Tezuka, Y. Nose, M. Fujii, and M. Atobe, "A low power, small, electrostatically-driven commercial inkjet head," in *Proc. IEEE Microelectromechan. Syst.*, Heidelberg, Germany, Jan. 1998, pp. 63–68.

[9] K. Ishihara, C. F. Yung, A. A. Aýon, and M. A. Schmidt, "An inertial sensor technology using DRIE and wafer bonding with interconnecting capability," *J. Microelectromechan. Syst.*, vol. 8, pp. 403–408, Dec. 1999.

[10] N. V. Deshpande, "Significance of inertance and resistance in fluidics of thermal ink-jet transducers," *J. Imaging Sci. Technol.*, vol. 40, no. 5, pp. 396–400, Sept./Oct. 1996.

[11] H. P. Barder and M. A. Lardon, "Planarization by radio-frequency bias sputtering of aluminum as studied experimentally and by computer simulation," *J. Vac. Sci. Tech.*, vol. A3, no. 6, p. 2167, Nov./Dec. 1985.

[12] P. A. Torpey, "Prevention of air ingestion in a thermal ink jet device," in *J. Imaging Sci. Technol., 4th Int. Congr. Advances Non-Impact Printing Technologies*, Springfield, VA, 1988, pp. 275–284.

[13] V. Ziebart, O. Paul, U. Münch, J. Schwizer, and H. Baltes, "Mechanical properties of thin films from the load deflection of long clamped plates," *J. Microelectromechan. Syst.*, vol. 7, pp. 320–328, Sept. 1998.

[14] M. O'Horo, J. O'Neill, E. Peeters, and S. Vandebroek, "Micromachining technology for thermal inkjet applications," in *Proc. Sensor Expo.*, Detroit, MI, 1997, pp. 275–279.

[15] Y. Watanabe, T. Mineta, S. Kobayashi, and K. Shibata, "The microassembly technique for a 3D single crystalline silicon structure using a polyimide/chromium cantilever," *Trans. IEE Japan*, vol. 119-E, no. 4, pp. 236–241, 1999.

[16] M. Simbo, K. Fukukawa, K. Fukuda, and K. Tanzawa, "Silicon-to-silicon direct bonding method," *J. Appl. Phys.*, vol. 60, p. 2987, 1986.

[17] G. Wallis and D. I. Pomerantz, "Field assisted glass-metal sealing," *J. Appl. Phys.*, vol. 40, pp. 3946–3949, 1969.

[18] A. C. Lazma, H. Jakobssen, and R. Puers, "The effect of the anodic bonding on the electrical characteristics of the p-n junctions," in *Transducers 99, Tech. Dig. Papers*, Sendai, Japan, 1999, pp. 1416–1419.

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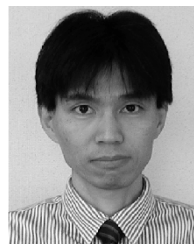

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