

## INTERMEDIATE COATING IC1-200

### Description

Intermediate Coating IC1-200 is a polysiloxane-based spin-on dielectric material, which is used primarily in the planarization of a topography of integrated circuits in multilevel metal techniques. IC1-200 is applied as a dielectric in a permanent or a partial etchback mode. Mechanical and electrical properties of IC1-200 are superior to those of other spin-on glass materials on the market. IC1-200 is also utilized as an intermediate layer in the trilayer resist technique and as a protective layer for plastics and metals.

### Advantages of IC1-200 over other commercial spin-on glass materials:

- Shelf life exceeding 5 years at room temperature storage
- Relatively low dielectric constant
- Lower tensile stress of the cured IC1-200 film
- Lack of silanol groups after curing at 400°C
- Superior film thickness uniformity
- Superior adhesion to polymeric and metallic surfaces
- Compatibility with resist coaters thus making application of dedicated SOG coater unnecessary

### Properties

|   |                     |
|---|---------------------|
| ◆ Solids Content (%)  | 7.2                 |
| ◆ Principal Solvent   | n-Butanol           |
| ◆ Appearance  | clear liquid        |
| ◆ Content of Particles (particles/mL)                       | <50 @ $\geq 0.2\mu$ |
| ◆ Absolute Filtration ( $\mu\text{m}$ )                     | 0.1                 |
| ◆ Coating Characteristic                                    | striation-free      |
| ◆ Spin Coating Thickness (nm) (3000 rpm, 40 s spin coating) |                     |
| 200°C bake, 60 s  | 200                 |
| 200°C bake, 60 s, 400°C bake in nitrogen, 30 minutes        | 170                 |
| ◆ Index of Refraction                                       |                     |
| 200°C bake, 60 s  | 1.41                |
| 200°C bake, 60 s, 400°C bake in nitrogen, 30 minutes        | 1.34                |

### Electrical Parameters

Process conditions: 3000 rpm spin coating, 400°C bake in nitrogen for 30 minutes

|  |                      |
|--|----------------------|
| ◆ Breakdown Voltage (MV/cm)              | 3                    |
| ◆ Volume Resistivity (ohms-cm)           | $5 \times 10^{13}$   |
| ◆ Surface Resistance (ohms / $\square$ ) | $> 2 \times 10^{12}$ |
| ◆ Dielectric Constant                    | 4.5 @ 10kHz          |
|  | 3.8 @ 1MHz           |
| ◆ Dissipation Constant                   | 0.05 @ 10kHz         |
|  | 0.2 @ 1MHz           |

### Mechanical Parameters

Process conditions: 3000 rpm spin coating, 400°C bake in nitrogen for 30 minutes

|   |                 |
|---|-----------------|
| Tensile Stress (dynes / $\text{cm}^2$ ) | $2 \times 10^8$ |
|---|-----------------|

## Processing

Application: Smoothing spin-on dielectric on top of the polysilicon pattern.

- ◆ Spin coating of a wafer with the IC1-200 applied directly on top of the preoxidized polysilicon pattern or on top of the reflowed BPSG at 3000 rpm for 40 s.
- ◆ 100°C bake on a hot plate for 60 s.
- ◆ 200°C bake on a hot plate for 60 s.
- ◆ 850°C bake in nitrogen for 30 minutes.
- ◆ Deposition and reflow of BPSG if a procedure calls for it.
- ◆ Patterning and etching of vias.
- ◆ Deposition, patterning and etching of the first level metal.

Application: Smoothing spin-on dielectric in a partial etchback mode for the multilevel metal.

- ◆ Deposition of the 100 nm thick silicon dioxide by the CVD on top of the first level metal.
- ◆ Spin coating of a wafer with the IC1-200 at 3000 rpm for 40 s.
- ◆ 100°C bake on a hot plate for 60 s.
- ◆ 200°C bake on a hot plate for 60 s.
- ◆ Repetition of coating and baking cycles if a procedure calls for it.
- ◆ 400°C bake in nitrogen for 30 minutes.
- ◆ Partial etchback of the IC1-200 and silicon dioxide in the RIE reactor using a mixture of CHF<sub>3</sub> and oxygen. The etchback is completed when the IC1-200 remains only at the foot of steps and in recessed and narrow areas of wafer topography.
- ◆ Deposition of the 800 - 1000 nm thick silicon dioxide by the CVD.
- ◆ Patterning and etching of contact vias.
- ◆ Deposition, patterning and etching of the second level metal

Application: Smoothing spin-on dielectric in a permanent mode for the multilevel metal.

- ◆ Deposition of the 100 nm thick silicon dioxide by the CVD on top of the first level metal.
- ◆ Spin coating of a wafer with the IC1-200 at 3000 rpm for 40 s.
- ◆ 100°C bake on a hot plate for 60 s.
- ◆ 200°C bake on a hot plate for 60 s.
- ◆ 400°C bake in nitrogen for 30 minutes.
- ◆ Deposition of the 800 nm thick silicon dioxide by the CVD.
- ◆ Patterning and etching of contact vias.
- ◆ Resist removal in a solvent-based resist stripper or in an oxygen plasma.
- ◆ 400°C bake in nitrogen for 30 minutes.
- ◆ Contact cleaning with the RIE using a gas composition and process conditions sufficient to remove 10 nm of aluminum.
- ◆ Contact cleaning with the argon sputter etching at a relatively low power to avoid gate damage. Process conditions should be selected to remove an equivalent of 10 - 20 nm of silicon dioxide.
- ◆ Deposition of 100 - 200 nm of titanium.
- ◆ Deposition of aluminum.
- ◆ Patterning and etching of the second level metal.

## Handling Precautions

Intermediate Coating IC1-200 is a flammable liquid and should be kept away from heat, sparks, and open flames. Avoid breathing vapors. Use product with adequate ventilation. Avoid contact with eyes, skin, and clothing. Wear chemical goggles, rubber gloves, and protective clothing. Accidental contact sites should be washed immediately.