Necessity of Chemical Edge Bead Removal in Modern Day Lithographic Processing

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ABSTRACT:

Some form of edge bead removal (EBR) is one of the standard requirements for a lithographic process. Without any intervention, resist may accumulate at the edge of the wafer at up to several times the nominal thickness of the resist. In addition to this edge bead, the resist is likely to wrap around the wafer contaminating the backside of the wafer as well. It's needless to say that such a condition would present a significant contamination risk not only for the resist track and the exposure tool but for process equipment outside of lithography as well. Two not necessarily exclusive strategies have been used in the past for edge bead removal. One is topside chemical EBR where solvent is dispensed on the edge of the wafer as the wafer is rotated immediately after coating, and the other method is where a ring of exposed resist is formed by subjecting the resist on the outer edges of the wafer to a broadband exposure; also know as wafer–edge exposure (WEE). The advantage of the chemical method is that it will remove the photo resist but also the organic anti-reflective coating (ARC), which is not photosensitive. The disadvantage of this method is obvious as any latitude in tool tolerances or imperfections on the wafer will result in solvent dispense to the undesirable areas of the wafer. While the optical method is much cleaner, its main disadvantage is that it will not remove ARC.

As the feature size and die size shrink, there is less and less repairable redundancy on modern semiconductor chips. An observed effect in our manufacturing facility has been an increased sensitivity to tool imperfections and a quantifiable level of yield loss due to solvent splashing for the 140nm generation. Accounting for the fact that the ARC layer is generally an order of magnitude thinner than the resist layer, yield-maximizing setup of edge bead removal for one lithographic layer and complete removal of topside chemical EBR is discussed in detail in this paper as well as the extension of the same principle to maximize yield at other layers.

Keywords: resist, arc, edge bead, chemical EBR, optical WEE, yield, splashing, defectivity

1. INTRODUCTION

One detrimental aspect of the coating process is that the rotational speed necessary to produce a layer of practical resist thickness is insufficient to overcome all attraction of the superfluous resist to itself and to the underlying substrate [1, 2]. Instead, resist tends to wrap around the backside of the wafer and accumulate at the edge as the centrifugal force pushes the material outwards (as illustrated in Figure 1) [1, 2, 3].

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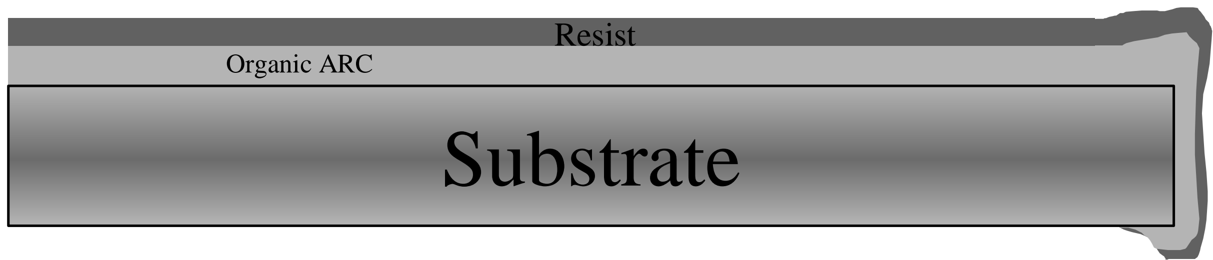


Figure 1: As an artifact of the coating process, resist tends to wrap around the edge of the wafer and accumulate there up to several times the nominal resist thickness [2]

Presence of the edge bead can lead to contamination problems on the coater cup and on other plates during subsequent processing on the track. Accumulation of the material on the edge of the wafer can also disturb patterning ability on the extreme edge of the wafer and wafer handling within the exposure tool, as well as cause erroneous leveling readings during exposure. Presence of the edge bead is also undesirable for subsequent processing and especially for the fabs with clamped etch system. Also, presence of the material on the backside not only increases the probability of higher number of hot spots but also has the potential to contaminate a number of tools outside of the area during upstream processing.

Due to all of the undesirable effects, most lithographic processes employ some type of edge bead removal. Three common types of EBR include backside rinse to remove backside contamination, optical edge exposure (for photosensitive material) and precise topside chemical removal (for either resist or other soluble material). Processes described here contained all three forms of EBR whereas the optical wafer edge exposure (WEE) setup was for a slightly wider coverage than the chemical component. Summary of the topside EBR process is shown in Figure 2.

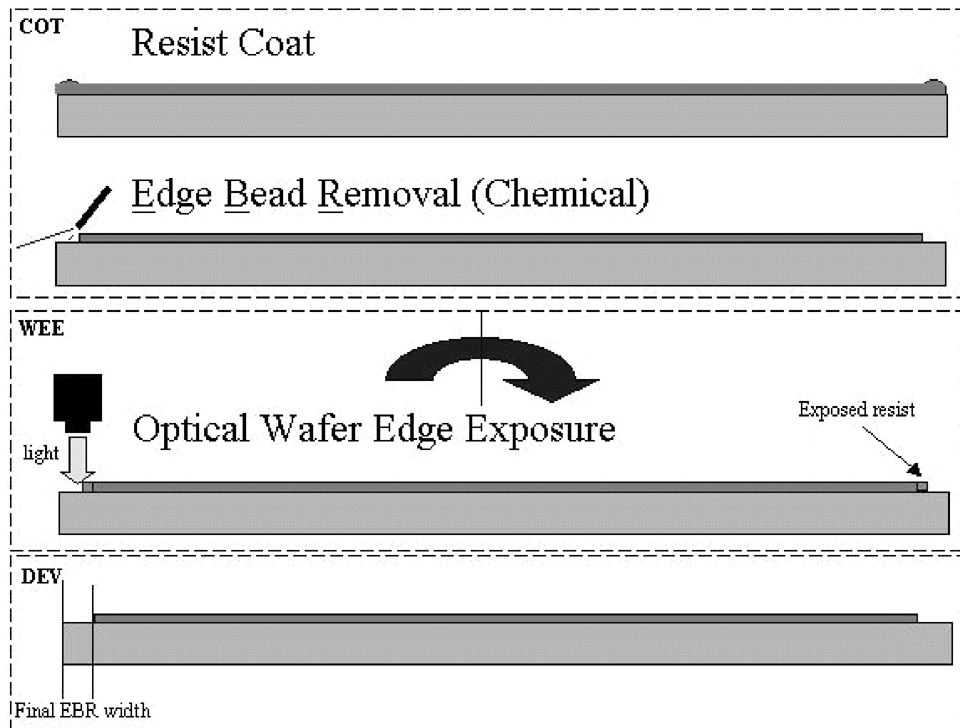


Figure 2. Description of the front-side EBR setup [1]

2. PROBLEM DEFINITION

Historically, most lithography processes within Infineon Technologies-Richmond were setup for 4.5 mm yield edge exclusion and 3.5 to 4.0 mm EBR without much problem. Difficulties started once the yield zone exclusion was changed to less than 2.0 mm [1]. As a result, EBR coverage had to be changed to be between 1.0 and 1.5 mm from the edge of the wafer, which with existing toolset tolerances, made it extremely difficult to process the material without frequently encountering defectivity problems. Most of the defectivity problems encountered were caused by solvent splashing due to a number of causes, which will be detailed in later sections. A typical defectivity signature encountered is shown below in Figure 3.

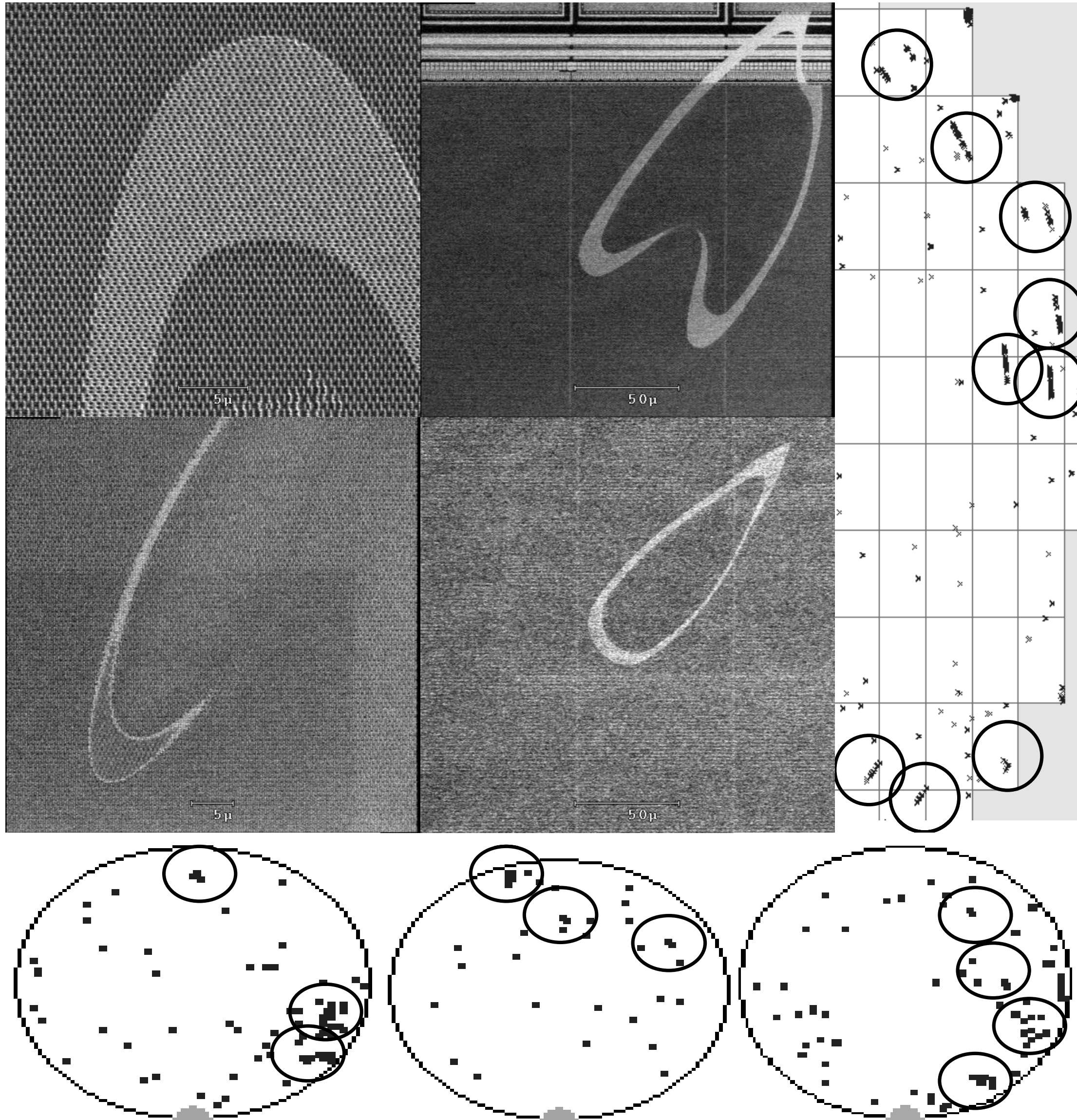


Figure 3. Typical defectivity signature from EBR splashing

At any given layer, yield loss caused by splashing was less than a fraction of a percent and was thus in itself not too great. However, the cumulative yield loss once all litho layers are combined was of course much greater and that is without even including the effects of less than infrequent excursions with the EBR setup. Even still, the overall yield loss was less than a percent. The biggest operational loss from continuous struggle with splashing was in expending tremendous engineering and technician time in dealing with the frequent occurrences and in manufacturing downtime for fixing each instance of the problem.

3. EQUIPMENT OPTIMIZATION

In addition to the generic track setup, the equipment group optimized a number of specific items that could cause splashing if not setup correctly. During the initial installation of a TEL track by the supplier a standard set of specifications are used to setup the coat modules. At Infineon we have optimized several of these specifications to control defectivity, chemical costs and availability.

3.1 Wafer Centering

The repeatability of placing wafers on the spin chuck accurately is very important not only to coating performance but also to chemical edge bead removal (EBR), and the backside rinse steps. The design of the picettes on a TEL ACT 8 Track demands that there must be some small amount of clearance around the edge of the wafer and the pincette fingers. Although this distance is small the Semi standard of a 200 mm wafer can be 200 mm +/- 0.25 mm and this gives a minimum clearance or movement of 0.5 mm. When setting up the hand off from the pincette to the spin chuck it must be remembered that the wafer will move forward in the pincette and this should be compensated for. The software will also allow you to designate pincette # 3 to hand off only to the spin modules cutting down on any variability. This setup becomes very important when the EBR width comes close to the wafer notch and wafer edge, any miss adjustment will disrupt the solvent stream on every revolution and can cause splashing or misting.

3.2 Airflow

The coat module exhaust setup is very important as it has an influence on both coating uniformity and the removal of contaminants from inside the coater cup module. Apart from the coating uniformity aspect we have found that if we do not clean the exhaust manifolds on a regular basis a significant build up of resist dust can accumulate altering the exhaust flow inside the unit.

When the exhaust is restricted or blocked the EBR and backside rinse streams can cause a misting effect inside the cup that can be transferred back onto the wafer. The same effect has been seen with resist spheres being deposited back onto wafers due to poor exhaust and lamina flow setup.

3.3 Flow Rates

EBR flow rates are checked during the PM cycle and our data shows that they do not change significantly although any air in the dispense lines can cause the stream to be interrupted and give some false readings. As long as the start of dispense is as far off the edge of the wafer as possible, any spluttering at the start will not come in contact with the wafer. The backside rinse setup is also checked on the PM cycle using the TEL glass wafer to ensure that the solvent path moves correctly towards the edge of the wafer and there is sufficient flow to move around the wafer edge and clean any residual resist.

Setting up the angle and height of the EBR needle can be a challenging and on several tools we have used a high-speed camera to understand the relationship between the two. One thing we did not expect to find was that some of our coat cups had small dents or cuts on the inside rings due to a wafer breakage or wear and tear. This caused some of the EBR to be deflected back towards the wafer instead of down the side of the cup. To better understand this we numbered every

part of the cup and logged which parts were in which Tool at any one time. This allowed us to back track any excursion and inspect the cup integrity of the cup parts.

3.4 Troubleshooting Tools

Making equipment adjustments once instances of splashing were reported was difficult because of the many causes and possible contributions. Furthermore, it was hard to separate occasional isolated incidence of splashing (as some level of splashing will always be encountered) with real instances when adjustments could significantly improve tool conditions. One invaluable tool that was used in optimizing the chemical EBR was the use of high-speed camera. Many effects such as those of solvent flows or wafer centering are impossible to tell via naked eye once the wafer is in full rotation. The high-speed camera allows engineers to examine events occurring within very small fractions of a second in a frame-by-frame manner thus more easily determining root cause of any instance of splashing. One significant finding is the splashing resulting from the interaction of the solvent stream with the wafer notch. As the topside chemical EBR width was narrowed to less than 1.5mm, this reduced the margin between the solvent stream and the notch. Any wafer placement slightly out-of-center resulted in the notch passing through the solvent stream and causing uncontrolled splashing. Examples of splashing are shown in Figures 4-6 below.

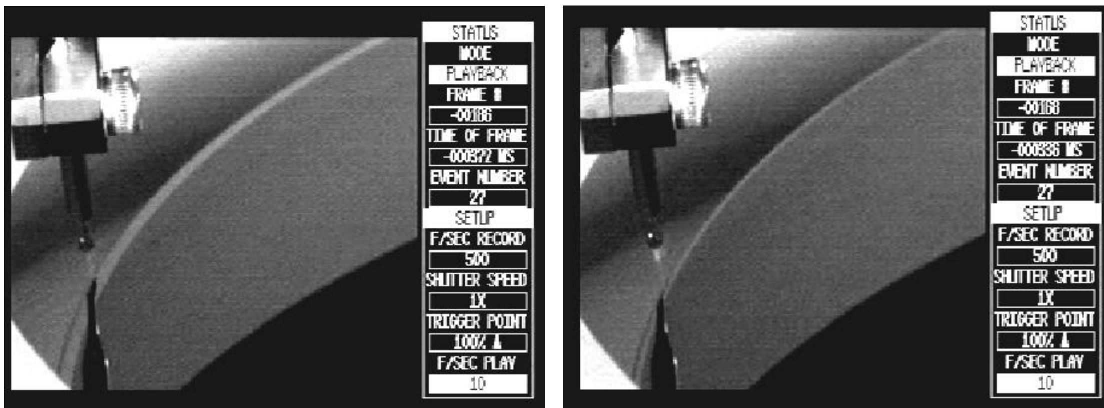


Figure 4: Wafer centering problem detected using high-speed camera

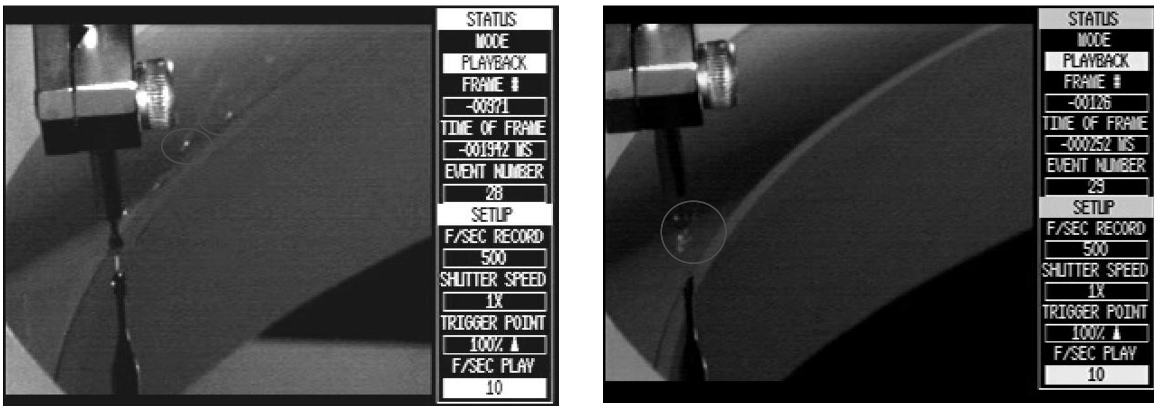


Figure 5: Isolating instance of splash back with the use of high-speed camera

Figure 6: Instance of splashing during nozzle retraction

4. PROCESS FIXES

Once all of the equipment fixes were made and significant defectivity problems still present, the major intent behind process fixes was to decrease reliability on chemical EBR.

4.1 Meeting 2 mm Yield Capability

Several years ago major efforts across all functional areas were started at Infineon Technologies Richmond in order to move the wafer edge exclusion to 2.0 mm and thus increase the functional number of die out with a minimal investment [1]. From the resist-processing standpoint, this entailed several major efforts including elimination of chemical EBR where possible or minimization of its effects on product. Thus wafer edge exposure (WEE) was used to clear out resist on the edge of the wafer for all but the thickest resists used in production. Furthermore, the use of the WEE was extended to enable step-to-edge printing by opening the scribe region as well to enhance topography and pattern density for subsequent CMP steps.

4.2 Backside Rinse

With the complete elimination of topside solvent EBR, one critical concern remains. Is the wafer bevel clean of resist and BARC? Many semiconductor-processing tools use some sort of handling technique that contacts the wafer bevel. In the case that resist or BARC is remaining on the bevel, this leads to contamination throughout the line and increased defectivity. To solve the problem, the backside solvent rinse must be optimized to clean the wafer bevel. Figure 7 shows (A) a standard BARC/resist coating with topside chemical EBR and wafer edge exposure compared to (B) the same process without topside chemical EBR. Note that in (B), delineation can be see where the bevel is cleaned.

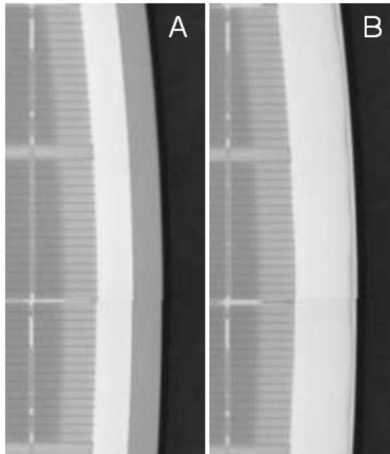


Figure 7: Comparison of BARC/resist process with (A) and without (B) topside chemical EBR
(wafer-edge-exposure is used in both)

Many factors contribute to the efficiency of the backside rinse for cleaning the wafer bevel. These factors can be divided into three categories; tool set-up parameters, process parameters, and chemical parameters. The tool set-up parameters will vary depending on the coater track used. These include, but are not limited to, dispense nozzle locations, dispense angle, and dispense flow rate. The primary process parameters are rotation speed during backside rinse, process time, exhaust flow rate, and bevel geometry. These first two categories contribute to the physical challenge of applying the solvent to the wafer bevel. The third category of parameters is the influence of the chemicals being used. The dissolution rate of the resist and BARC in the chosen solvent will affect the time required for the cleaning step. Also, the affinity of the solvent to the resist and BARC will affect the level to which the solvent wraps around the bevel.

4.3 WEE Optimization

Wafer Edge Exposure (WEE) unit, where possible, allows for a much better control of edge bead removal because the width and uniformity of the exposed edge bead can be calibrated and controlled to a better extent than the chemical edge bead removal process. Furthermore, use of WEE allows for non-problematic coverage of the notch region whereas the chemical process inevitably will be problematic due to its mechanical nature. WEE use also allows future extendibility of the same concept to smaller edge exclusions that may be necessary down the road (1.5 or 1.0 mm).

In addition to the advantages of the improved accuracy and control, the use of WEE was also beneficial in that it allowed for solving of certain process problems. Without step-to-edge patterning in all regions of the wafer, CMP polish rate non-uniformities were resulting in drastic Shallow Trench Isolation (STI) step-height thickness variations, which in turn affected yield. By placing WEE stripes in areas of the wafer that were not covered with step-to-edge, these CMP uniformities were significantly improved. Likewise, WEE usage enabled us to use step-to-edge coverage in the regions of the wafer that we previously could not do so because of issues such as scribe readability. Combining step to edge coverage with a WEE stripe aimed at clearing the scribe region, the problem was successfully solved.

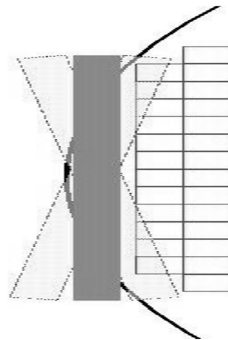
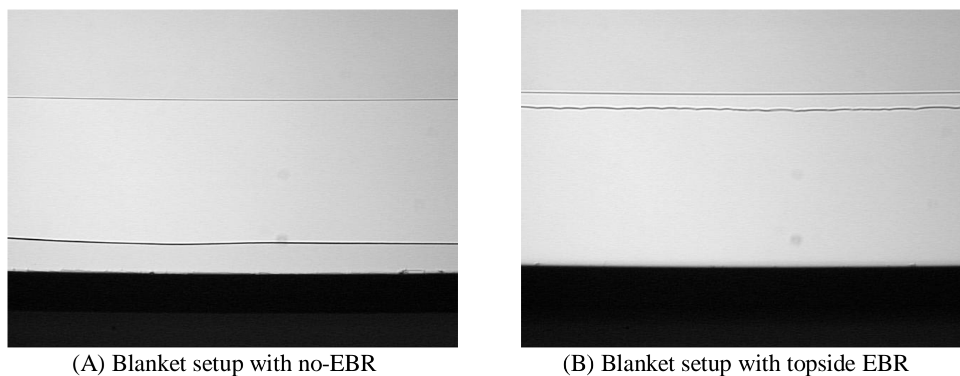


Figure 8: Showing tight control requirements on WEE

The only major disadvantage of the use of WEE compared to chemical processing has been the requirement for tighter tolerance of the placement accuracy in both the process recipes and maintenance activities. Figure 8 conceptually shows the situation encountered for one of our parts where WEE stripe control is crucial. In this situation, we are only able to control placement of the stripe to within 0.5 degrees.

4.4 Qualification Requirements

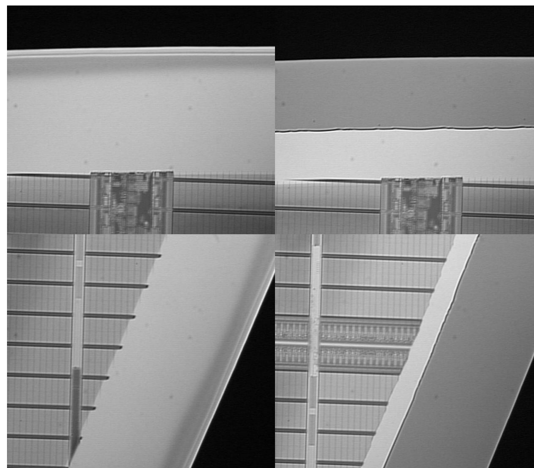
Qualification efforts for extending the use of optical WEE and decreasing the use of chemical processing necessitated a lengthy qualification plan. As part of the qualification, the effects were first examined on bare wafers as shown in Figure 9.



(A) Blanket setup with no-EBR (B) Blanket setup with topside EBR

Figure 9: Eliminating topside EBR

Next the effect was examined on product. Of specific interest was the thickness of the remaining material and its proximity to good die. Also, patterning ability in the region was examined to see if there were any noticeable effects between the two groups (see Figures 10 and 11).



Without topside EBR With topside EBR

Figure 10: Optical comparison of EBR efficiency

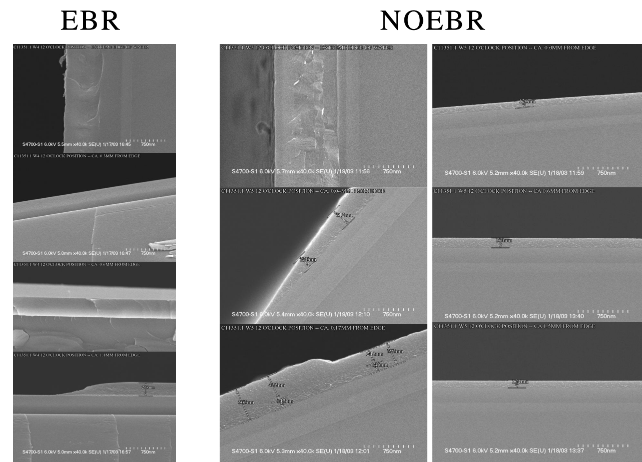


Figure 11: X-section comparison of thicknesses

As shown in Figure 10, there is an obvious edge visual difference between the two processes. As the figure shows, WEE unit was obviously successful in removing the resist but significant layer of BARC still remained. Furthermore, the BARC layer was cleared-away at the proximity of 0.8 mm from the edge of the wafer and then rapidly accumulated on the extreme edge. This was a potential concern so cross-sectional analysis was performed in order to establish the material thickness profile on the edge of the wafer. These results shown in Figure 11 relieved some of the concerns as although BARC thickness on the order of 3X nominal thickness was seen at a distance of 0.1 mm from the edge, this thickness diminished very rapidly to zero at a distance of 0.04 mm from the edge. Thus, the backside rinse seemed capable of assuring that no material wrapped around the edge of the wafer.

Based on this information, several split lots were run through the un-clamped etch step. Endpoint and edge CD data were examined in detail and no statistical differences were found. Effects of change in EBR were obviously not a concern after the etch and subsequent remaining resist strip step. Following positive results, a 20% pilot was instituted on one tool for an extended period of time. During this time frame, no adverse effects such as any undesirable inline trends or increase in defectivity trends were observed for the tool in question or for the material in question. The second pilot was then extended into production converting all of the material running on that tool to the new process. Performance of this tool was compared to the other tools and only a significant improvement via decreased defectivity for this cluster was observed. Based on positive results, the pilot was extended to 20% of the material running on the other tools. Once the pilots were completed, there were no inline differences seen but only a remarkable improvement in defectivity and a small improvement in yields (due to previous yield loss from splashing). While the implementation of the first layer was very conservative because it was first such experience for us, subsequent layers were implemented much quicker and often even skipping the pilot phase altogether. The cumulative effect of improved EBR setup has been to significantly reduce the number of defectivity problems and to cumulatively add small fraction to yield at every step. Furthermore, cost savings were also realized since chemical EBR is now used only in fraction of the processes.

5. CONCLUSION

This paper discussed challenges of extending conventional edge bead removal techniques into the future as edge exclusions shrink to less than 2.0 mm. Defectivity problems encountered with tighter tolerances on the EBR processing were discussed and numerous equipment techniques offered to diagnose and improve EBR setup including the use of high-speed video camera. The necessity of chemical EBR was challenged for most modern lithographic applications and our experience shown where we have de-qualified topside chemical EBR almost entirely resulting in significant savings from reduced defectivity, improved yields, and reduced chemical costs across multiple layers.

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