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Low temperature GaAs/Si direct wafer bonding

M. Alexe, V. Dragoi, M. Reiche and U. Gösele

GaAs-Si low temperature. bonding fas been achieved using spin-on-glass as the intermediate layer. Interface energies of 1.7J/cm2 were obtained after thermal annealing at only 200°C. The interface energy is sufficiently high to allow thinning of the GaAs wafer down to 5-10um.

Introduction: Much scientific interest is being focused on the monolithic integration of GaAs optoelectronic devices with high speed silicon integrated circuits. The main requirement for the integration is to combine high quality single crystalline GaAs layers with silicon substrates. A GaAs/Si heterostructure would have the advantage of combiig the properties of both Si and GaAs in order to achieve the integration of GaAs optoelectronic devices with silicon signal processing devices on the same chip and also dissipating higher power than those on GaAs substrates due to the three times higher thermal conductivity of silicon [1]. The main objective is to produce a material system in which a thin GaAs layer showing bulk quality is monolithically integrated on an Si substrate. Usually, GaAs layers are fabricated on Si substrates by heteroepitaxial growth. The formation of anti-phase boundaries, 4.1% lattice mismatch between GaAs and Si, and low temperature epitaxy are major problems encountered in this case [2 ,3] Most of these problems can be avoided by using the direct wafer bonding (DWB) technique [4 5] to fabricate GaAs/Si heterostructures. By DWB it is possible either to transfer a singlecrystalline (100) GaAs layer on an Si substrate using for instance hydrogen implantation induced splitting [6], or to integrate silicon in the GaAs technology by transferring silicon layers on GaAs wafers [7]. The most difficult problem which has to be overcome in bonding GaAs to Si is the large difference between the thermal expansion coefficients (TECs) of Si and GaAs (the TEC of GaAs *is* almost twice that of Si) [8, 9]. This usually leads to debonding at thermal annealing over 160°C and, as a consequence of such a low annealing temperature, the surface energy is limited to 0.20 – 0.30J/m2 [10]. The thermal mismatch problem can in principle be solved by using silicon on sapphire wafers [11] instead of simple silicon wafer, but costs would be drastically increased. In this Letter a technique for the direct bonding of to Si using a spin-on glass (SOG) intermediate layer is proposed. Glass layers have already been used as intermediate layers in the DWB of Si/Si or GaAs/GaAs. In comparison with glass layers obtained by vapour deposition methods such as chemical vapour deposition [12], e-beam evaporation [13], or by spray pyrolysis [14], spin-on deposition is very simple and, moreover, SOG is a standard SiO_2 glass extensively used in microelectronic processing and does not contain electronically undesirable elements such as sodium [12] or dopants such as boron [7, 12, 14].

Results: 4" silicon (100)-oriented wafers (525µm thick) were first covered with SOG layers by spin-on deposition of a commercially available silicate glass (SOG) precursor (Fiitronics, Inc.). Thin films with thickness ~3700Å were obtained by spinning the precursor at 3500rpm for 35s. After spinning, the SOG layers were baked for 5 rnin on a hot plate in air at 150°C. The SOG-coated Si wafers were then room temperature bonded with semi-insulating 4" GaAs (100) wafers (625µm thick). The wafers were bonded using a microcleanroom setup in a cycle consisting of 2 min rinsing with deionised water followed by spinning at 3000 rpm. The bonding quality is mainly determined by the quality of the SOG layer; particles, inclusions or layer inhomogeneities lead usually to unbonded areas. The surface energy of the room temperature bonded wafers measured by the crack opening method was in the range 0.3 – 0.5 J/m^2. This value is very high compared with the surface energy in the case of silicon-to-silicon hydrophilic bonding (0.1 – 0.15 J/m^2). The room temperature bonded wafers were subsequently subjected to a thermal annealing for 10h at temperatures ranging from 200 to 225°C. After the annealing at 200°C the GaAs/Si surface energy reached $1.7 J/m^2$. Fig. 1 shows the infrared transmission image of the GaAs/Si wafer pair after annealing at 200°C. A further increase in temperature to 225°C does not damage the bonding but also does not increase the energy as is shown in Fig. 2.

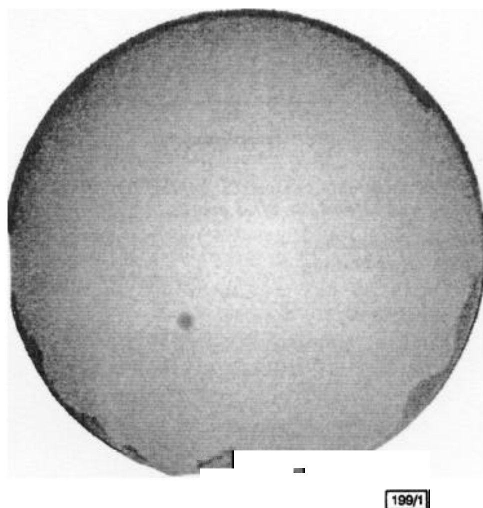

Fig. 1 Infrared transmission image of 4" GaAs wafer bonded to Si via SOG and annealed at 200°C for 10h

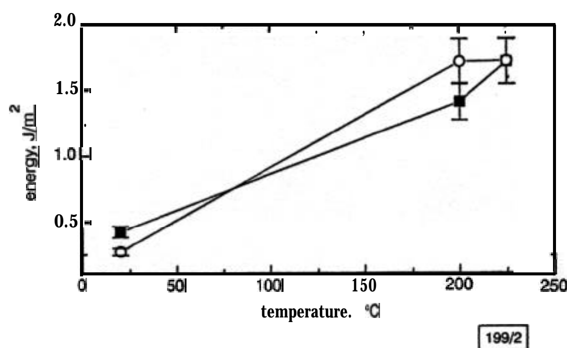

Fig. 2 *Surface energy of two different GaAs/Si bonded samples after annealing at two different temperatures*

The bow of the GaAs/Si bonded wafers was measured during the annealing after the room temperature bonding during ramping up and as well during ramping down of the temperature. Fig. 3 shows bow values increasing up to 500µm at 200°C. During the cooling down to room temperature the bow comes back to zero without any hysteresis and without affecting the bonded interface. To determine the maximum temperature at which the GaAs/Si wafer pair can be annealed, a second run of the bow measurement was performed after cooling the sample to room temperature. The bow increase follows exactly the initial path and at ~280°C the wafers debond and/or shatter. By thinning one of the wafers down to some tens of micrometres, depending on the fmal purpose either the integration of GaAs into silicon technology or integration of Si into the gallium arsenide technology can lead to an increase in this maximum temperature limit to values of 450°C. 6 x 6mm^2 samples were cut and submitted to tensile stress testing. The average energy determined from the tensile stress tests for an SOG bonded GaAs/Si sample annealed for 10h at 200°C is 22MPa. Atomic force microscopy and scanning electron microscopy (not shown here) revealed that the SOG film broke during the tensile stress test and did not debond from either Si or GaAs. This can demonstrate the suitability of the SOG layer as an 'adhesion layer'. Cross-section transmission electron microscopy (TEM) investigations into the GaAs/Si bonded interface shown in Fig. 3 revealed a good GaAs-glass bonded interface. 4" GaAs/Si bonded samples fabricated as described above were submitted to grinding followed by chemical mechanical polishing (CMP). The GaAs wafers were grinded down to 30 – 40µm and polished down to 10µm confirming that the achieved interface energy is sufficiently

high to allow even the harsh mechanical processing of the bonded wafers.

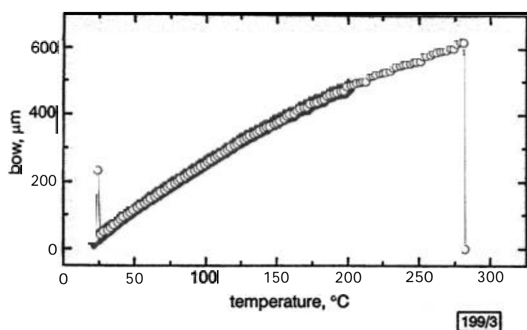

Fig. 3 Bow *measurements of GaAs/Si bonded sample during initial thermal annealing and second run after cooling*

■ initial thermal annealing
0 second run after cooling

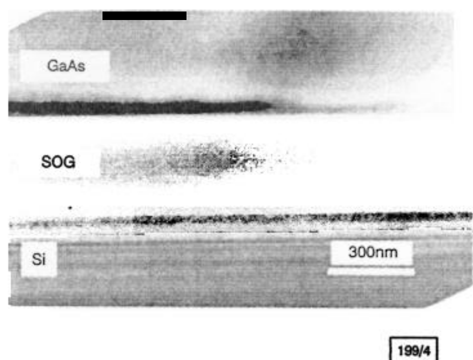

Fig. 4 Typical cross-section TEM image of GaAs/SOG/Si interface after annealing at 200°C for 10h

Conclusions: We have demonstrated a true low temperature bonding process using commercially available spin-on glass layers as an intermediate layer. SOG bonding is a simple, versatile and electronically clean process and it can be applied for gallium arsenide-to-silicon bonding and as well for silicon-to-silicon bonding. The interface energy achieved for SOG bonded GaAs/Si is -1.7 J/m^2 after annealing at 200°C.

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Adaptive MLSE receiver: hybrid of per-survivor processing and tentative decision MLSE

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An adaptive maximum likelihood sequence estimation (MLSE) receiver is proposed that employs both per-survivor processing (PSP)-MLSE and tentative decision (TD)-MLSE by selecting one of them based on the instantaneous signal-to-noise ratio (SNR). Since the instantaneous SNR varies according to the channel, the proposed hybrid receiver can automatically control its complexity relative to the channel environment. Computer simulation results indicate that when compared with the PSP-MLSE, the proposed receiver can significantly reduce complexity with only a slight degradation in performance.

Introduction: Recently, an algorithm [1] that can reduce the computational complexity of per-survivor processing-maximum likelihood sequence estimation (PSP-MLSE) [2, 3], a powerful technique for sequence detection in uncertain environments, has been introduced. In contrast to PSP-MLSE, in which estimates of unknown parameters are made for every survivor in the trellis paths, the algorithm presented in [I] selects the N best survivors at each detection step and then only estimates parameters for those N survivors, where $1 \leq N \leq Q$ and Q denotes the number of trellis states. The remaining Q – N survivors are assigned the parameter estimate associated with the best survivor. Accordingly, this algorithm, which will be referred to as N-survivor processing (NSP)-MLSE, is able to make a compromise between complexity and performance by adjusting the parameter N. NSP-MLSE is equivalent to PSP-MLSE when N = Q, and TD-MLSE [4, 5] when N =

In this Letter, we propose an alternative approach to reducing the complexity of PSP-MLSE. The proposed method, called hybrid-MLSE, employs both PSP-MLSE and TD-MLSE by selecting one of them based on a comparison of the instantaneous SNR with a threshold. Owing to the fact that the instantaneous SNR varies according to the channel, in hybrid-ML%, automatic control over the complexity relative to the channel environment is possible, without the need to adjust the threshold. As a result, hybrid-MLSE offers a compromise between complexity and performance more efficiently than NSP-MLSE. Computer simulation results indicate that a hybrid-MLSE receiver can significantly reduce computational complexity, while maintaining a performance comparable to that of a PSP-MLSE receiver.