

Patterning of light-extraction nanostructures on sapphire substrates using nanoimprint and ICP etching with different masking materials

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Abstract

Sapphire nanopatterning is the key solution to GaN light emitting diode (LED) light extraction. One challenge is to etch deep nanostructures with a vertical sidewall in sapphire. Here, we report a study of the effects of two masking materials (SiO_2 and Cr) and different etching recipes (the reaction gas ratio, the reaction pressure and the inductive power) in a chlorine-based (BCl_3 and Cl_2) inductively coupled plasma (ICP) etching of deep nanopillars in sapphire, and the etching process optimization. The masking materials were patterned by nanoimprinting. We have achieved high aspect ratio sapphire nanopillar arrays with a much steeper sidewall than the previous etching methods. We discover that the SiO_2 mask has much slower erosion rate than the Cr mask under the same etching condition, leading to the deep cylinder-shaped nanopillars (122 nm diameter, 200 nm pitch, 170 nm high, flat top, and a vertical sidewall of 80° angle), rather than the pyramid-shaped shallow pillars (200 nm based diameter, 52 nm height, and 42° sidewall) resulted by using Cr mask. The processes developed are scalable to large volume LED manufacturing.

Keywords: LED light extraction, sapphire nanopattern, SiO_2 mask, nanoimprint, ICP etching

(Some figures may appear in colour only in the online journal)

1. Introduction

A critical challenge in light emitting diodes (LEDs) is high light extraction. For GaN LEDs on sapphire substrate, the GaN active layer has larger refractive index ($n_{\text{GaN}} = 2.5$) than the substrate ($n_{\text{sapphire}} = 1.7$) and air, hence having a severe light trapping problem. The trapped light does not only wastes energy, but also heats up LEDs and greatly shortens LED lifetime, both substantially increasing lighting cost. One way to improve light extraction is to pattern the nanostructures on the sapphire substrates, which also improves the GaN epitaxial crystal quality [1]. However, it is a challenge to etch a sapphire substrate to the desired shape and depth in the required nanoscale, since sapphire is mechanically strong (e.g. hard) and chemically resistant [2]. For example, previous sapphire patterning in nanoscale suffers from inaccessibility

to deep patterning, because (a) in wet etching, the etching is anisotropic and the etched profile is determined by r -plane ($1\bar{1}02$), which has the lowest wet-etching rate and thus pins the sidewall slope angle at 57° [3, 4]; and (b) in dry etching, the etched depth is limited by the etching mask erosion and lateral etching [5–7]. In addition, for the commonly-used metallic etching mask, it usually causes micromasking problem: the metal fragments sputtered by plasma get re-deposited on the etching area and form an etching mask for the underneath material, creating undesired grass-like nanostructures [8] and (the remaining metal) contaminating subsequent fabrication steps [9]. Therefore, there is a need for developing a process of patterning nanostructures in sapphire that have deep and vertical profiles, and for further investigation of the etching masking materials and etching processes.

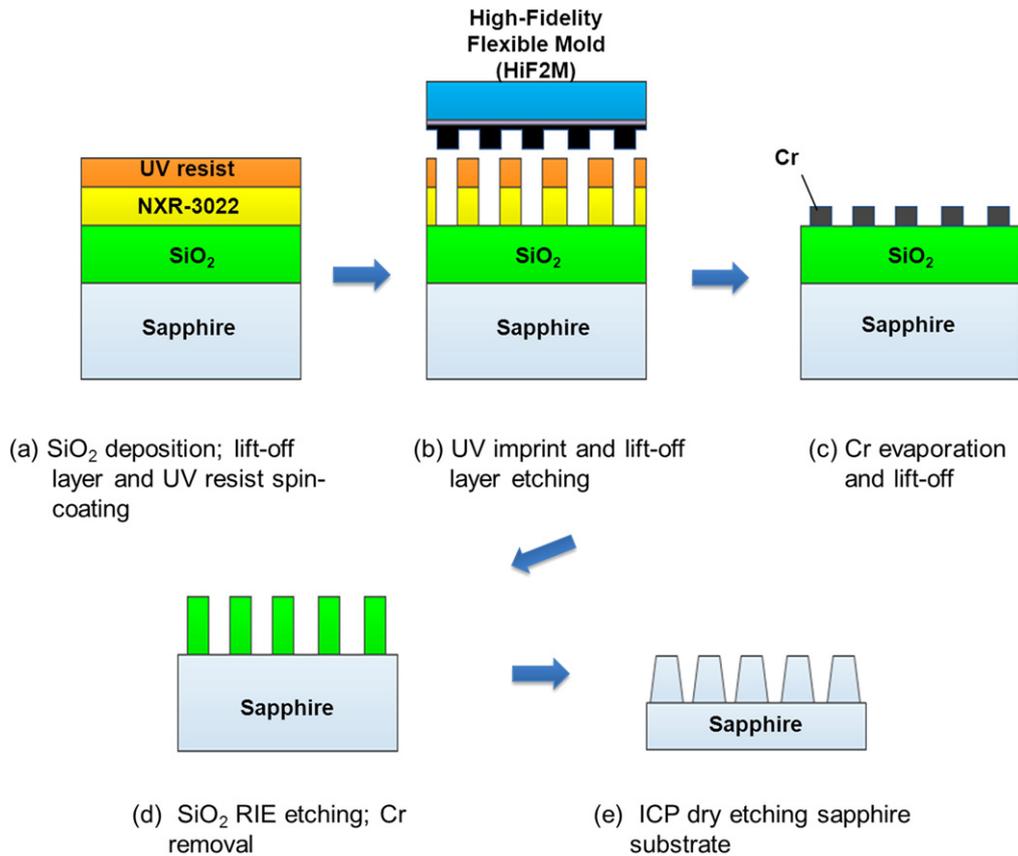


Figure 1. Key steps of sapphire nanopatterning with SiO₂ mask: SiO₂ mask patterning by nanoimprint lithography, and ICP dry etching.

Here we present a study of the sapphire etching by two mask materials (SiO₂ and Cr), and different etching processes. SiO₂ and Cr are two representative materials for dielectric mask and metal mask commonly used in nanofabrication. With SiO₂ masking, we achieved a sapphire nanopillar array with 200 nm pitch, 122 nm pillar diameter, 170 nm height and a sidewall angle of 80°, which shows significantly deeper etching with steeper pillar sidewall than the previous wet etching and dry etching.

2. Experiments

In our experiments, *c*-plane (0001) sapphire wafers were used for nanopatterning tests, as a typical substrate in GaN LED manufacturing. The sapphire nanopatterning has two key steps: (a) patterning the nanostructure etching mask on the sapphire substrate, and (b) inductively coupled plasma (ICP) etching of the sapphire substrate using the etching mask.

2.1. Patterning of nanostructured etching masks

Both the SiO₂ mask and the Cr mask were patterned by nanoimprint lithography. The SiO₂ mask patterning has five key steps (figures 1(a)–(d)): (1) deposition of a 350 nm thick SiO₂ layer on sapphire by plasma-enhanced chemical vapor deposition at 250 °C, using a mixture of silane (SiH₄) and nitrous oxide (N₂O); (2) UV nanoimprint lithography of

nanoholes with 200 nm pitch and 125 nm diameter in a spin-coated 145 nm thick UV resist, which is on top of a spin-coated 140 nm thick lift-off layer, baked at 130 °C for 5 min); (3) deposition and lift-off of a 20 nm thick Cr; (4) etching of SiO₂ using fluorine-based chemicals in reactive ion etching (RIE), transferring the Cr nanopattern to the SiO₂ layer, forming SiO₂ nanopillar on the surface of sapphire substrate, and (5) removing the Cr.

The nanoimprint mold we used in the UV nanoimprint is a High-Fidelity Flexible Mold (HiF2M) with a 3-layer structure [10]: thick flexible polyethylene terephthalate substrate, bonding layer, and a high modulus surface layer carrying 200 nm pitch 125 nm diameter nanopillar patterns. Its flexible substrate enables uneven surface patterning, and the hard surface layer ensures high fidelity patterning with sub-10 nm resolution. The UV nanoimprint used 20 s UV exposure at the density of 40 W cm⁻² for a full resist curing.

For the Cr mask fabrication, it has only two steps: (1) nanoimprint with a double layer resist (145 nm thick UV resist on top of 250 nm lift-off layer), and (2) deposition and lift-off Cr of 160 nm thick. Since it is very difficult to dry etch a thick Cr layer to form ~100 nm patterns, a lift-off method is applied here.

2.2. Etching of sapphire substrates

The sapphire substrate was etched using chlorine-based ICP with an etcher (SAMCO RIE-200iP, figure 1(e)) [11]. Both

Table 1. The original inductively coupled plasma (ICP) etching recipe used before optimization.

BCl ₃ flow rate (sccm)	Cl ₂ flow rate (sccm)	Ar flow rate (sccm)		
40	10	5		
Inductive power (W)	DC bias power (W)	Chamber pressure (Pa)	Substrate temperature (°C)	
600	150	2	70	
Sapphire etching rate (nm min ⁻¹)		SiO ₂ mask erosion rate (nm min ⁻¹)		
46		12		

Table 2. Optimized ICP etching recipe. This recipe is optimized by choosing etching conditions with highest η factor shown in figure 6.

BCl ₃ flow rate (sccm)	Cl ₂ flow rate (sccm)	Ar flow rate (sccm)		
40	10	5		
Inductive power (W)	DC bias power (W)	Chamber pressure (Pa)	Substrate temperature (°C)	
200	150	5	70	
Sapphire etching rate (nm min ⁻¹)		SiO ₂ mask erosion rate (nm min ⁻¹)		
24		2		

SiO₂ and Cr etching masks were tested under the same ICP etching condition for comparison. The key processing parameters such as the etching rate, etching profile, and mask erosion were measured.

First, we started from testing a common sapphire etching recipe (table 1): BCl₃ and Cl₂ mixed at a combination of 80%/20%, with 10% additional Ar flow, which gives the maximum etching selectivity; BCl₃ species breaks Al–O bond in the form of creating volatile boron–oxygen–chlorine compounds (e.g., BOCl) [12, 13], and Cl₂ serves as the main etchant for aluminum, forming high vapor pressure chlorides [14, 15]. Inductive power and DC bias power were set to 600 W and 150 W, respectively, with a stable chamber pressure of 2 Pa; the heated substrate at 70 °C also facilitated etching rate [16, 17]. Then we optimized the etching recipe to facilitate anisotropic etching by using different combinations of BCl₃/Cl₂ (10%/90%–100%/0%), different pressures (0.5–14 Pa), and different inductive powers (200–1000 W), while the total flow rate of chlorine-based gas, dc bias power, substrate temperature, and argon flow rate were fixed at 50 sccm, 150 W, 70 °C and 5 sccm, respectively. The details of the recipes and the results are summarized in table 1 (original recipe) and table 2 (optimized recipe).

3. Results and discussions

3.1. Etching masks

The scanning electron microscope study of the fabricated mask array shows (1) the thickness of the fabricated mask is 350 nm for SiO₂ mask (figure 2(a)), but only 120 nm for Cr

mask (figure 2(b)). The Cr mask thickness is less than the intended thickness of 160 nm due to the shadowing effect during Cr evaporation. Part of Cr deposited on the edge of the evaporation window formed by imprinted resist eventually closes up the window as evaporation continues (figure 2(c)) [18, 19]. The mask aspect ratio for SiO₂ and Cr are 3 and 0.9, respectively. (2) The sidewall slopes are also different: nearly 90° sidewall for SiO₂ mask (hence cylinder-shape), but 57° for Cr mask (hence pyramid-shape). The average mask diameter is 118 nm for SiO₂ mask, but 133 nm for Cr mask at its base. The sloped sidewall and pyramid shape of Cr mask is also due to the shadowing effect shown in figure 2(c), as the evaporation window keeps shrinking during Cr evaporation.

3.2. Sapphire ICP etching

The sapphire wafers with the SiO₂ and Cr masks were etched in the same ICP etching run, hence by the same etching recipes and conditions. The results show that the final etched profiles strongly depend upon the etching masks (figure 3). Using the SiO₂ mask and a 4 min etching, there is only 5 nm shrinking in SiO₂ mask average size (from original 118–113 nm, figure 3(a)), and the etched sapphire pillars have a uniform cylinder shape: 108 nm in height, 122 nm in diameter, and 80° sidewall angle (figure 3(b)). The 80° sidewall slope is, to our best knowledge, the highest achieved in etching sapphire nanopillars.

In contrast, using Cr mask and a 4 min etching, the Cr mask gets severely eroded (the mask diameter decreases from 133 nm to 36 nm, figure 3(d)), and the short sapphire pillars have pyramid shape: 52 nm height, 36 nm pillar top

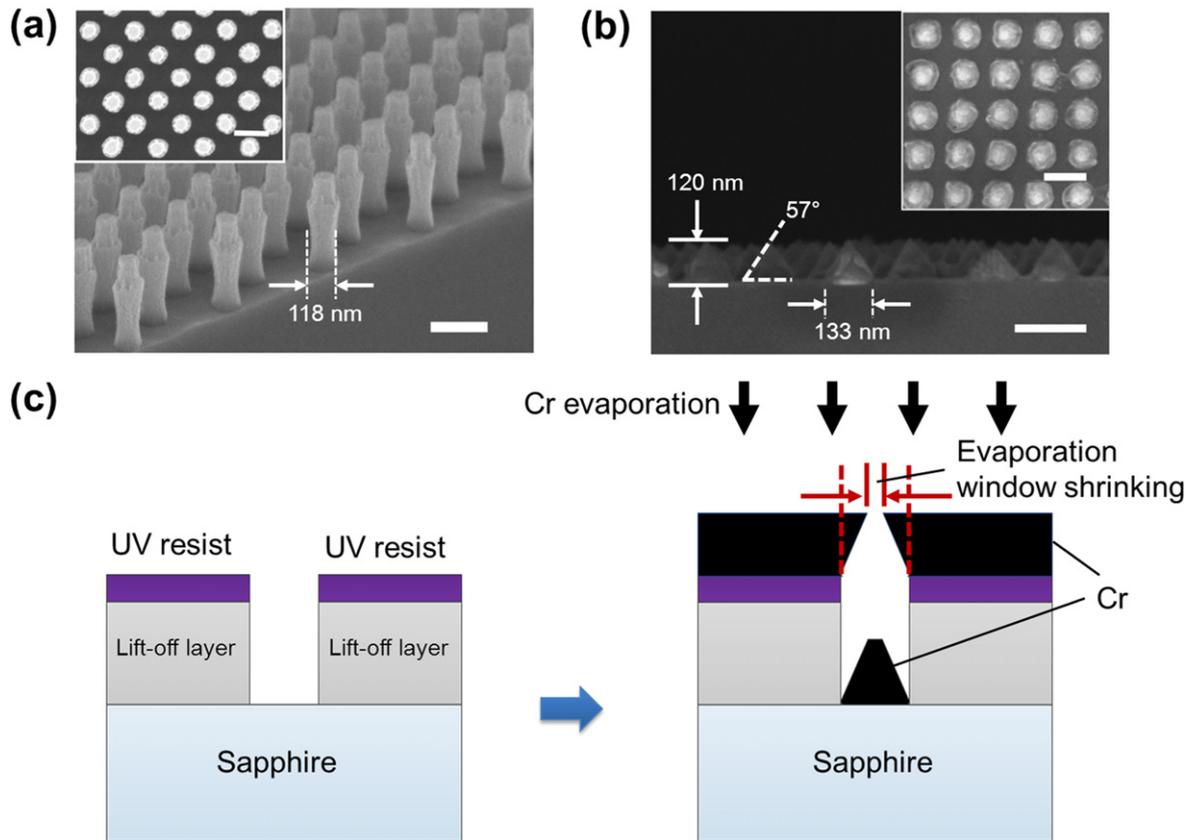


Figure 2 (a) SiO₂ nanopillar mask (tilt view), fabricated from RIE etching, and (b) Cr nanopillar mask (cross-section view), fabricated from evaporation-and-liftoff process (scale bar = 200 nm) (c) pyramid-shape Cr mask is formed by Cr shadowing effect during deposition. As Cr evaporation continues, the evaporation window eventually closes up, resulting in that Cr thickness is less than intended.

diameter, 200 nm pillar base diameter (the same as the pillar period), and 42° sidewall angle (figure 3(e)). The pillar height of 52 nm from Cr mask is only 48% of 108 nm from SiO₂ mask. The higher profile for SiO₂ mask is a result of the *c*-plane etching; for Cr mask, *c*-plane is quickly etched out due to the non-vertical etching, hence further etching stops. It is noted that the sidewall angle of nanopillars from SiO₂ mask (80°) is 38° higher than that from Cr mask (42°), which is a significant improvement in sapphire vertical etching.

Using the SiO₂ mask and a 7 min etching, the sapphire pillars are taller and remain near-perfect cylinder shape (170 nm in height, and the same 122 nm diameter and 80° sidewall angle as the 4 min etching) (figure 3(c)). This indicates again nearly no lateral mask erosion for chloride-based ICP using SiO₂ as mask. In contrast, using the Cr mask and a 7 min etching, the erosions in Cr mask and the sapphire nanopillars are so severe that all Cr masks were gone, and nearly no sapphire pillars left (figure 3(f)). This result means that Cr mask is not suited for masking deep and sharp etching on sapphire using chlorine-based ICP.

The low lateral erosion rate of the SiO₂ mask and the high erosion rate of the Cr mask are expected in chlorine-based chemistry, which is known to etching of metals like Cr, but much less has been studied on SiO₂ mask. Actually, there are two factors affecting mask lateral erosion: (1) mask

material reaction and (2) mask profile. Regarding the material effect, the chlorine in the gas mixture reacts with Cr to form chromium chloride, causing Cr mask to erode; chlorine barely affects the SiO₂ mask, leading to little erosion. On the other hand, regarding the profile effect, it is discovered that pyramid-shaped Cr mask is not favorable to the ICP etching. Originally, etching selectivity of Cr/sapphire can be as high as 5:1 [16]. However, for the pyramid-shaped Cr mask, selectivity is significantly lower (less than 1:2). Its low-sloped sidewall suffers from more plasma attacks than vertical sidewall, inducing fast erosion (figure 4(a)). The severe lateral erosion is worsened by the ions aberrant from the vertical direction that lead to lateral mask etching [20, 21]. Fast Cr mask erosion means the masking area at the end of etching is much smaller than that at the beginning, which is one of the major causes for low-sloped sapphire pillar profile. In contrast, SiO₂ mask with vertical sidewall shows little lateral erosion, as its sidewall is not directly exposed to vertically accelerated ions (figure 4(b)).

We define the mask erosion rate as the mask size reduction per minute during ICP etching. Our experiment based on recipe in table 1 indicates that, under all the etching conditions, SiO₂ mask stably achieved slower erosion rate and thus better profile than the Cr mask. Firstly, for ICP inductive power, figure 5(a)

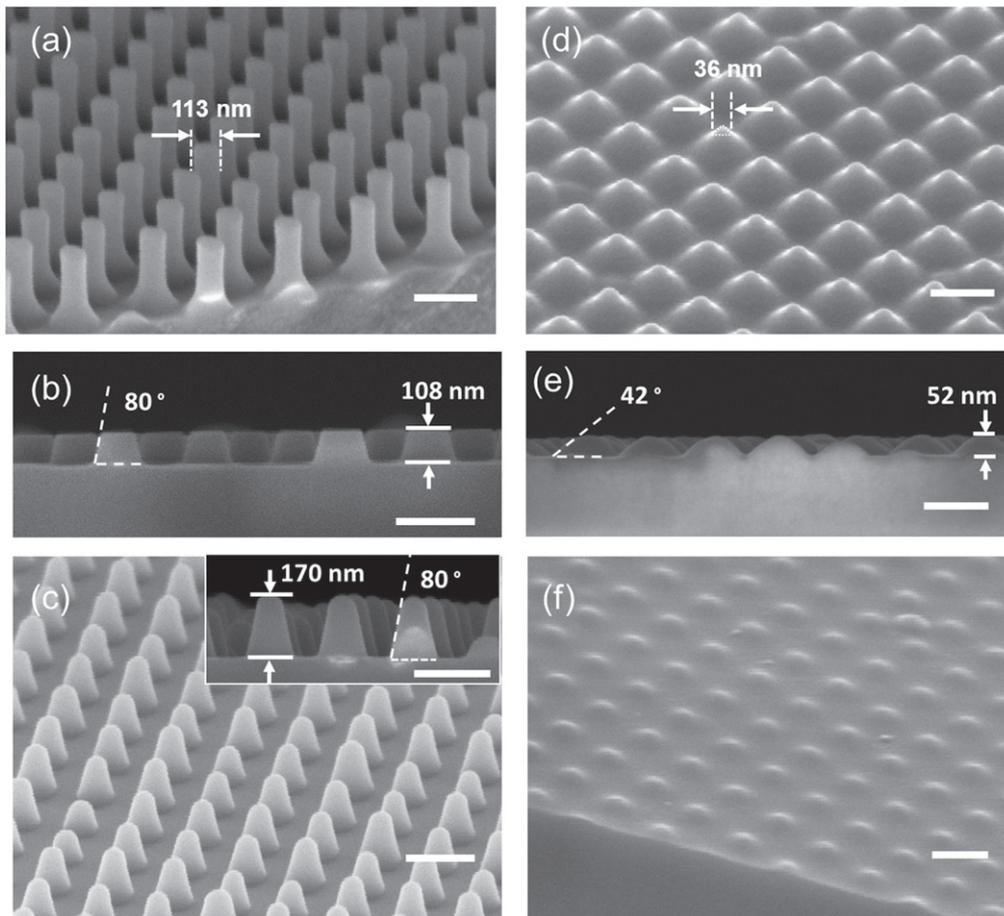


Figure 3. Sapphire etching result showing deep and vertical nanopillars from SiO₂ mask (left column, (a)–(c)), compared to Cr mask (right column, (d)–(f)). (a) SiO₂ mask after 4 min etching, showing little lateral erosion; (b) cross-section of etched pillars for 4 min etching masked by SiO₂; (c) final sapphire pillar profiles masked by SiO₂ mask after 7 min etching. (inset) cross-section view showing final sidewall angle of 80°; (d)–(f) sapphire etching masked by Cr under same etching process corresponding to (a)–(c), showing severely eroded Cr mask and no pillar structure formed. (Scale bar = 200 nm).

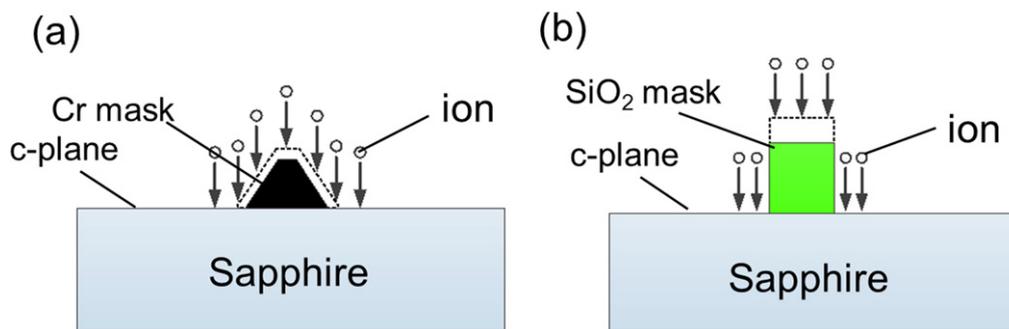


Figure 4. (a) For pyramid-shaped Cr mask, its sloped sidewall gets etched by ICP ions, inducing lateral mask erosion. (b) SiO₂ mask has vertical sidewall, effectively avoid sidewall etching and thus lateral mask erosion. (Dashed line represents mask profile before ICP etching.)

illustrates that erosion rate of SiO₂ mask is roughly three times smaller than Cr mask within a wide range of ICP inductive powers (200–1000 W). Secondly, as shown in figure 5(b), for chemical combinations of boron trichloride (BCl₃) and chlorine (Cl₂), Cr mask erodes very fast in chlorine environment (127 nm min⁻¹ for 90% chlorine environment); on the contrary, SiO₂ mask erodes stably slower over all the BCl₃/Cl₂ combination. Thirdly, for etching pressure, figure 5(c) shows erosion

rate as high as 148 nm min⁻¹ for Cr mask, while for SiO₂ mask it is <20 nm min⁻¹ under all pressures from 0.5 Pa to 14 Pa.

The slow erosion rate of the SiO₂ mask demonstrates that the SiO₂ has the flexibility to be used as mask under various etching conditions. In contrast, the Cr mask has to stay in extremely low pressure in a chlorine-free environment for less mask erosion.

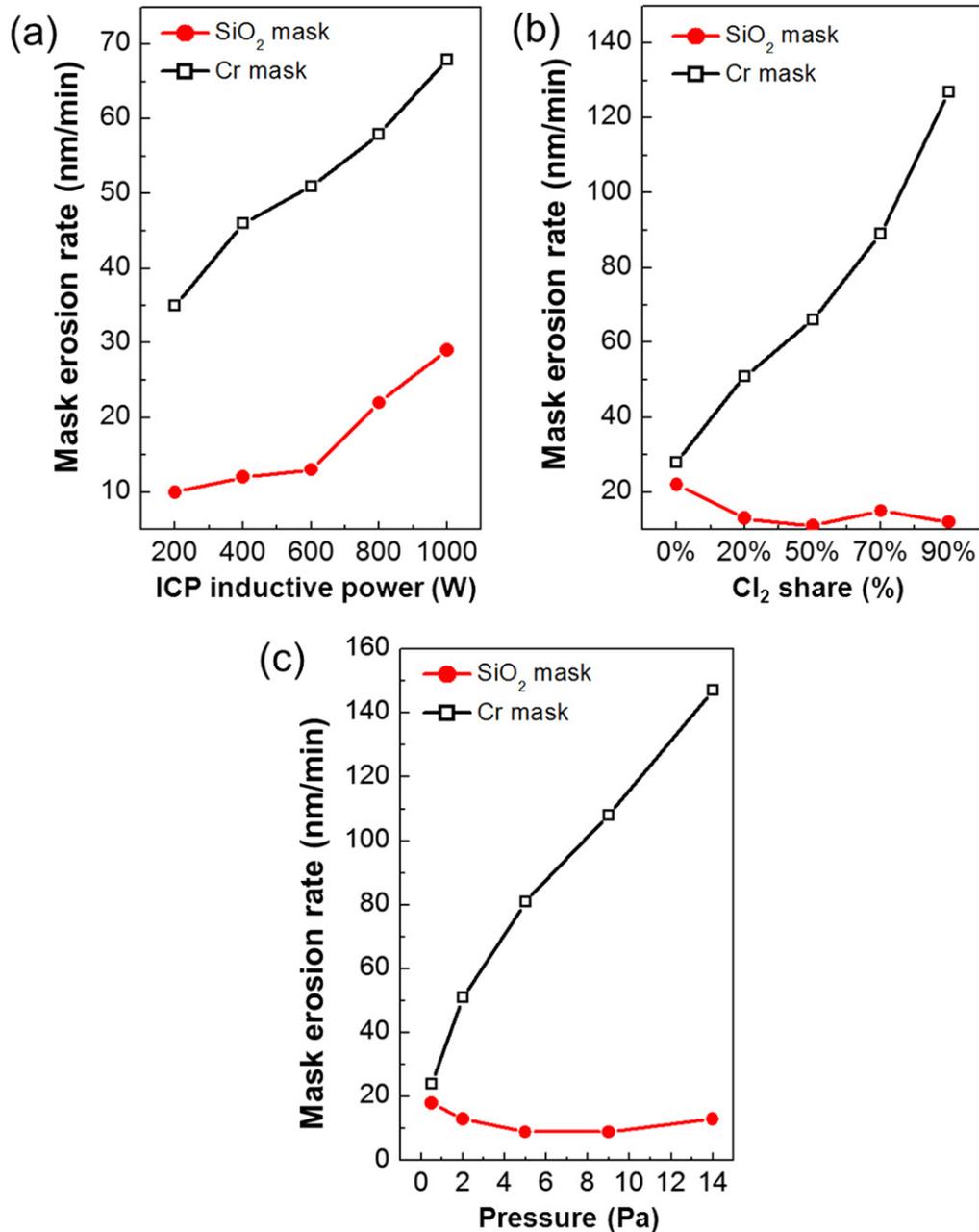


Figure 5. SiO₂ mask erodes much slower than Cr mask under all etching conditions, including different (a) ICP inductive powers, (b) gas combinations, and (c) chamber pressures.

3.3. Etching recipe optimization

The final sapphire etching recipe (ICP power, chemical mix, and ICP pressure) was optimized by maximizing the ratio of sapphire etching rate to the SiO₂ mask erosion rate, which is defined as the effective etching factor η :

$$\eta = \frac{\text{Sapphire etching rate}}{\text{SiO}_2 \text{ mask lateral erosion rate}}. \quad (1)$$

In general, for a deep vertical etching profile, it is desired to achieve a higher sapphire etching rate while limit the mask lateral erosion, corresponding to a high η . Hence we define the best etching condition to be the one with the highest factor η .

Firstly, η increases monotonically with decreasing ICP power, having the maximum η when ICP power is at its lowest tested level of 200 W, mainly because low power has the slowest mask erosion at this level (figure 6(a)). Secondly, for a 600 W ICP power, the combination of 80% BCl₃/20% Cl₂ mix reaches the highest η (figure 6(b)), indicating that majority of BCl₃ significantly accelerates sapphire etching without inducing further mask erosion. Thirdly, for 600 W ICP power and 80% BCl₃/20% Cl₂ mix, η reaches its maximum at an ICP pressure of 5 Pa (figure 6(c)). This shows that etching with either too low or too high pressure is not favorable. At high pressure end, sapphire etching rate decreases, because ion energy greatly drops in high density plasma due to the severe ion scattering [22, 23]. At low pressure end, the mask erosion lowers η .

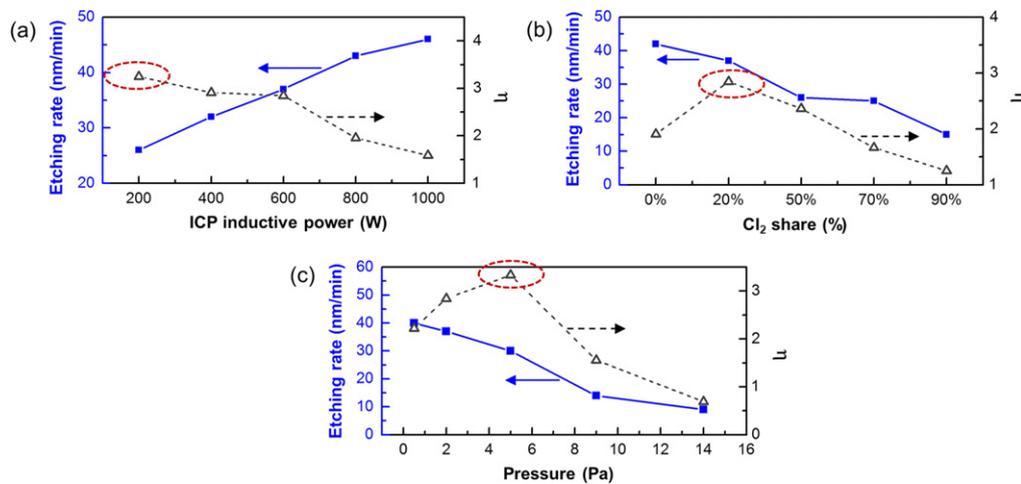


Figure 6. Measured sapphire etching rate and factor η by sweeping (a) ICP inductive powers, (b) gas combinations, and (c) chamber pressures. (Solid line) sapphire etching rate; (dashed line) factor η values. Dash-circled are the highest η values. Etching recipe was optimized by choosing the etching condition with the highest η .

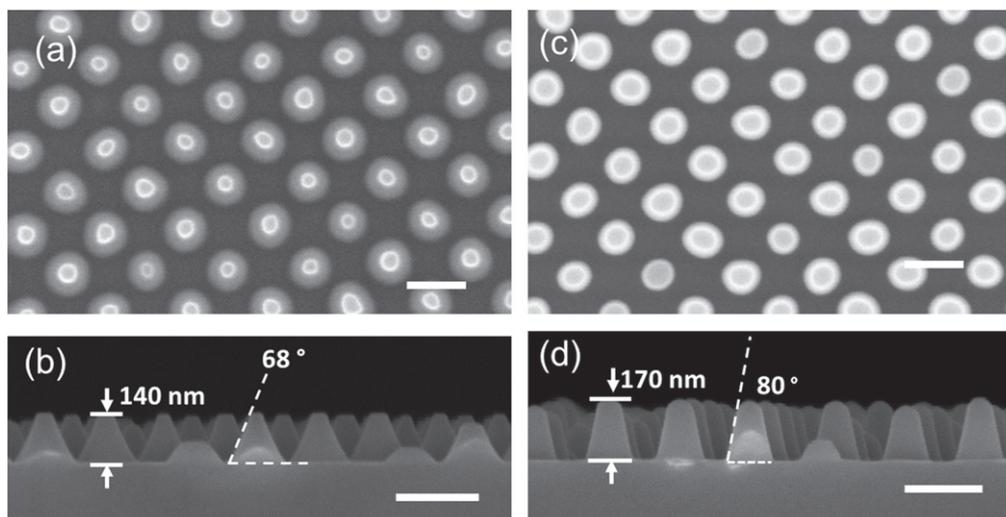


Figure 7. (a),(b) Sapphire pillars etched by the original etching recipe before optimization (table 1), forming sapphire nanopillars with sidewall angle of 68°; compared to (c), (d) sapphire pillars etched by optimized etching recipe (table 2), showing sidewall angle of 80° (scale bar = 200 nm).

The optimized ICP etching recipe with the etching condition with highest η , picked from figure 6, is: BCl (80%)/ Cl_2 (20%), 5 Pa chamber pressure, and 200 W ICP power (summarized in table 2). Before optimization, pillar sidewall angle was 68° (figure 7(b)). Using the optimized recipe, 80° sapphire sidewall angle is achieved (figure 7(d)), with 12° improvement. The optimized recipe also reduces the mask erosion from original 12 nm min⁻¹ (figure 7(a)) to 2 nm min⁻¹ (figure 7(c)). The improved etching profile validates our previous optimization analysis: less ion density (lower inductive power) and lower ion energy (higher pressure) reduce the non-directional etching, thus forces vertical etching of sapphire and less lateral erosion to the mask.

4. Conclusion

We developed a sapphire nanopatterning method using nanoimprint, SiO_2 masking, and ICP etching to achieve sapphire nanopillars with vertical sidewall. By comparing the performance between Cr mask and SiO_2 mask in sapphire etching masking, we found that SiO_2 , which is compatible in common IC fabrication tools, is superior to Cr mask. SiO_2 mask is capable to achieve high sapphire nanopillars with vertical sidewalls. Its advantage over Cr mask is independent of etching conditions, suitable for a wide range of etching requirements. We optimized the etching recipe and achieved the highest reported sidewall angle of 80° in sapphire nanopatterning. The process developed here can be applied to

large volume manufacturing for future GaN LED light extraction applications.

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