Deep anisotropic ICP plasma etching designed for high volume MEMS manufacturing

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1. ABSTRACT

ICP plasma etching is gaining widespread acceptance as an enabling mirocmachining technology for advanced MEMS fabrication. Whereas this technology has shown a capability of delivering multiple novel applications for R&D, its acceptance by industry for high volume production has been limited. This acceptance into production will only occur when the plasma etching equipment with this technology offers the device performance, throughput, reliability, and uptime criteria required by a production facility. The design of the plasma etcher using this technology and the process capability it consequently delivers, has significant implications in making this a reality. Alcatel has been supplying such a technology to this MEMS industry for over 5 years and in the interim has evolved its product and process to make this technology production worthy. Alcatel's next generation etcher, the Alcatel 601E, offers multiple advantages to MEMS manufacturers in realizing their production goals.

This paper will present some of Alcatel's recent improvements to make the process suitable for production. The main improvements include the highest possible silicon etch rate in the industry (upto 10μm/min), very high aspect ratio (upto 90:1), very high mask selectivity to resist (upto 250:1) and to oxide (upto 1000:1), shallow to through-the-wafer etching with vertical sidewalls, etching silicon on-insulator structures with no undercut or notching, and process uniformity <+/- 5% across a wafer. Some results of this technology, as applied to the production of automotive sensors, will also be presented. The Alcatel system offers an improved version of the deep etch process licensed from Robert Bosch GmbH of Germany, along with a polymer –free cryogenic deep etch process on the same system. Alcatel's superior process results and a reliable production-oriented platform design offers high wafer throughput, better device performance, simplified process flow, process flexibility and high system uptime during its operation. Multiple industrial customers for high volume sensor manufacturing are adopting Alcatel's ICP deep etch technology.

2. INTRODUCTION

Production for Microelectromechanical systems (MEMS) devices is one of the key technology areas to revolutionize the 21st century. These devices consist of smart sensors and micro actuators integrated into electronic control circuitry. These broad ranges of applications are used in automotive, aerospace, bio-medical, computer peripherals and telecommunication industries. The deep silicon etching for MEMS applications is more complicated than IC applications. These are some comparisons between MEMS and IC deep silicon etching.

MEMS deep silicon etching

1. Different feature sizes and shapes
2. No equal spacing between different feature sizes and shapes
3. Silicon etch depths range from a few microns to a few hundred microns or through wafer.
4. Etching into a cavity or stop on oxide layer depends on device types.
5. Etching on polysilicon, epitaxial film or single crystal silicon
6. The devices have to perform for both electrical and mechanical functions

Current IC deep silicon trench etching

1. Typical same feature size and shape
2. Same spacing with same feature size and shape.
3. The silicon etch depth is typically < 20 microns except power device.
4. No etching into cavity or stop on oxide layer.
5. Etching on single crystal silicon.
6. The devices performs on electrical and no mechanical functions.

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7. Etch feature sizes range from a few mm to a sub-micron. 7. Etch feature sizes are sub-micron.

The etch requirements are very important in many areas, including profile control, CD loss, selectivity, minimal undercut with stop on oxide layer or no notching and high silicon etch rate. All of the specifications are key factors for MEMS production applications. The transition from wet etching to dry etching for MEMS is very similar to an early day of IC dry etching. The MEMS feature size is shrinking along with the devices that will transfer more and more to dry etching technique. The typical MEMS devices cost much less than IC microprocesser devices. Therefore, these MEMS production devices are very sensitive to every fabrication step that is associated with equipment cost. The MEMS devices have an advantage by borrowing many process technologies from IC fabrication and equipment. The MEMS fabrication can utilize the used or existing IC equipment for some process steps. However,with the deep silicon etching area it is more difficult to use a conventional IC type etcher. This is due to some constraints:

1. IC single crystal silicon deep etching has low etch rates, and low selectivity to oxide or photoresist masks.
2. The IC etch equipment cost is very high, along with the cost of using corrosive chemistry and associated facility costs of handling the corrosive environment.

Therefore, the decision making is very important to select the right etch equipment for production. One etch tool needs to perform both R&D and production functions. This will reduce the process transfer time from R&D to a production type tool and reduces the cost of having to purchase two types etch equipment (R&D and production). The ideal configuration is to select one tool for both requirements with minimal modifications.

3. EXPERIMENTAL

Silicon substrates P and N type, {100} orientation were used for this investigation. The wafer size ranges from 4" to 6" patterned with thermal oxide or positive photoresist materials. An Alcatel 601E system is used for this work. The major components of this 601E system include a process chamber, with atmospheric robotic transfer of wafers between atmospheric cassette to vacuum load lock. The second robotic arm in the vacuum transfer chamber picks the wafer from the load lock and moves it to the pedestal and into the process chamber. The RF power to plasma source is an independent control to the substrate RF power. The etching process is performed with a temperature control range from –20° C to + 30° C. The plasma source uses an Alcatel patented (HICP) high density inductively coupled plasma source ($>10^{11}$ ions/cm^3 in argon) with non corrosive fluorine based chemistry. A set of permanent magnets in the process chamber wall magnetically confines the plasma. A turbo pump is used in the process chamber backed up by a mechanical pump. The mask openings were etched by dry etching an oxide mask. The etch feature sizes range from sub micron to a few hundred microns. The etching profiles were determined by Hitachi SEM.

System description

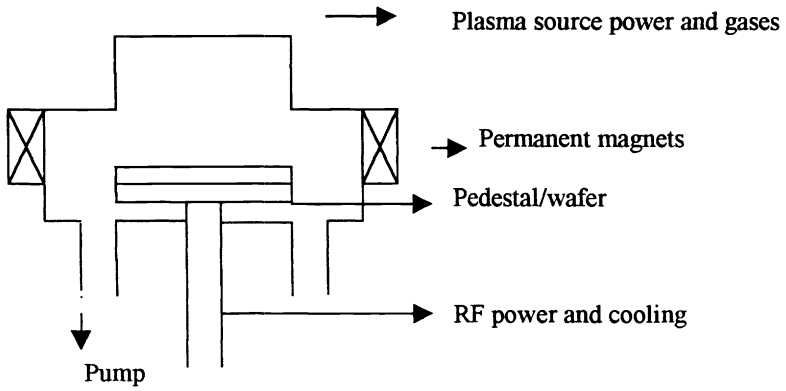

Fig.1 Schematic Diagram of the Alcatel process chamber.

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4. HIGH ETCH RATE

The high etch rate of bulk silicon is an important requirement for production throughput, when the device requires an etch depth beyond 50 microns to through wafer etching. Some applications have less stringent requirements on CD loss and profile angle on the larger feature sizes. There are process trade offs between etch rate and other requirements. In some situations the process trade off can be very minimal and maintain etch rates as high as 10 μm/min with a good profile control. The high etch rate in such processes is influenced by many things. It can separated into three major contributors:

1. Mask design and feature sizes on the wafer.
2. Etch process chemistry and parameter settings for the process recipe.
3. Etch system design of the process chamber and pumping.

4.1 Mask design and feature sizes on the wafer

The large feature sizes always etch faster than the small feature sizes. The percentage of exposed etching relative to masking material plays a key role in this high etch rate. A less amount of silicon exposed area in a mask design will result in high etch rate and better uniformity. The large feature size provides more etching species to etch the silicon material. Fig.2 demonstrates etch rate versus silicon exposed area on 4" silicon wafer.

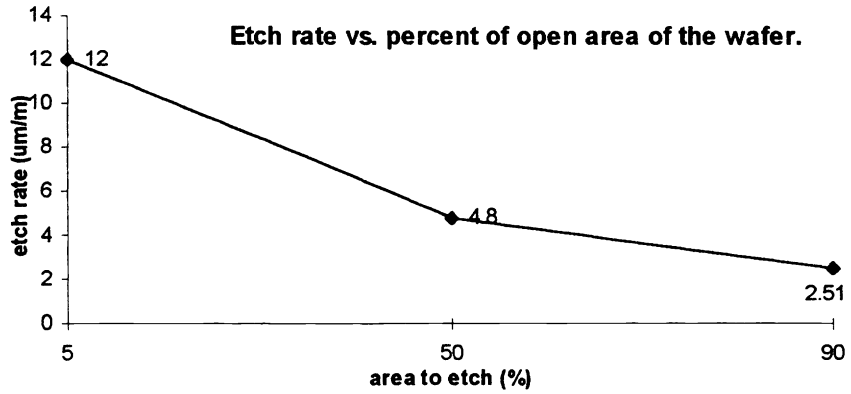

Fig.2 etch rate versus exposed silicon area on 4" silicon wafer

As a general rule on mask design, if it is possible, keep the exposed silicon area to masking material ratio less than 1:3. This will help etch rate and uniformity. Fig.3 shows the cross section of trench depth > 400 microns with etch rate > 10μm/min with good profile control on a 5" silicon wafer.

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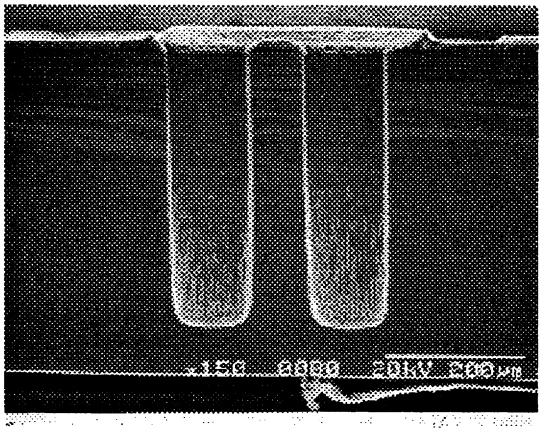

Fig.3 cross section of high etch rate > 10μm/min on 100 feature size with > 400 μm depth

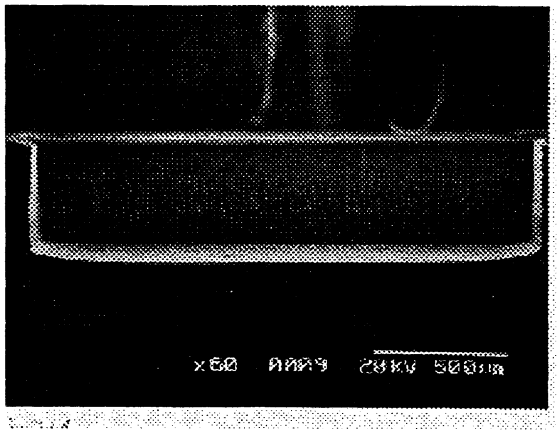

Fig 4. Cross section of a large open area with feature size 2mm and depth >500um. The exposed area is 60%, etch rate 5um/min. Despite the wider trench the etch rate is less than in fig. 3 due to a larger exposed area.

4.2 Etch process chemistry and parameters setting for process recipe

The correct gas chemistry is one of the keys for a high etch rate. This high silicon etch rate experiment uses SF_6 as a main etching gas. Superior properties and electronegativity of this SF_6 gas, with high thermal conduction caused by a disassociation reaction, enhance some of this high rate. Fluorine from SF_6 is the most dominant reactant[1]. Other gases can also be used such as CF_4, C_2F_6 Cl_2 HCl, HBr and etc. In the case of C_xF_y these gases are used for silicon etching. The silicon etch rate shows a lower etch rate than SF_6[2]. This suggests the carbon concentration atoms are deposited on the silicon surface. Oxygen can be used as an additive for removing the carbon as a volatile by-product of CO and CO_2. The majority of silicon is being etched by chemical etch instead of physical etch. This high etch rate is dominated by a chemical reaction rather then a physical reaction. Some physical (sputtering etch) etching occurred when substrate bias is applied to the wafer. As the etch rate of silicon with SF_6 is higher than that with C_xF_y gases, an accumulation of sulfur is less prominent than carbon. This indicated the sulfur could be easily removed by ion bombardment from biasing the substrate. Other parameter settings for the process recipe play an important role for high etch rate such as, plasma source power, pressure, gas flow, substrate bias, temperature and etc. Each parameter has its own influence on etch rate. Therefore, each parameter must be optimized by means of design of experiment (DOE) or other techniques to obtain an optimized condition for the final process recipe on high silicon etch rate. Source power is one of the major contributors to high etch rate as demonstrated in Fig.5.

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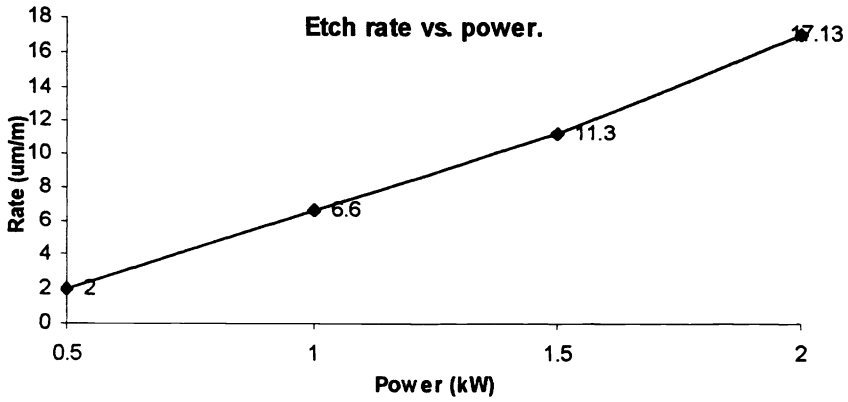

Fig. 5 silicon etch rate versus source power

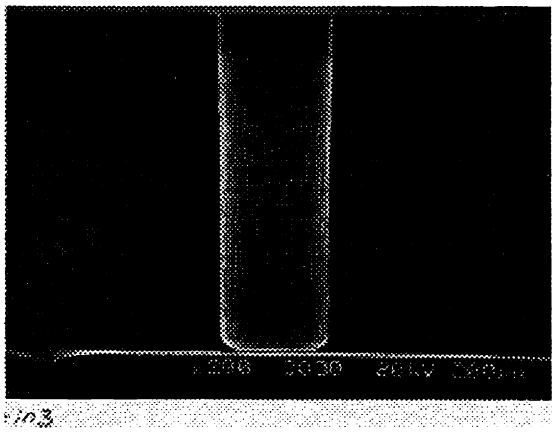

Fig. 6 high etch rate of near through wafer etching on large feature size.

4.3 Etch system design on process chamber and pumping.

Each etch process chamber has a uniqueness as its own design. The process chamber has many parts that will influence the etching performance. The plasma source efficiency plays a very important role on high etch rate, uniformity etc. Having a good ICP source design itself is not enough to achieve a high etch rate. Alcatel's process chamber has a unique design that is a result of many years of design experience. Alcatel has been a supplier of many generations of systems since the early days of dry etching from a planar etcher, RIE, ECR as well as different generations of ICP sources. The pumping conductance with correct configuration has an important role in this high etch rate process. The Alcatel turbo pump for this system is specially designed for dry etching. The objective in this vacuum pumping is to remove the byproducts from gas reactions on the wafer as quickly as possible and maximizing the conductance from the wafer to the pump. The etching is critically dependent on the reaction of gas molecules and reactive ions at the wafer surface. The amount of this energetic ions arrival rate and directionality of reactive gases determine the etch rate. The byproducts that are quickly removed from the wafer surface as the new fresh reactant arrive enhance this high etch rate. All of these unique parts are integrated into an Alcatel's etch system for the MEMS applications and it also can be applied to other industries such as semiconductor fabrication and power device applications.

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5. HIGH ASPECT RATIO ETCHING

With conventional wet chemical etching processes, the silicon is etched preferentially along a certain silicon crystal orientation and attainable aspect ratios are typically 10:1. The dry etching is not affected by the silicon crystal orientation and it has little affect on undercut. It depends mainly on control of the process parameters. Dry etching is capable of delivering much higher aspect ratios than wet etching and maintain a high etch rate with vertical profile control inside the trench. If device feature sizes are tightly packed, the undercut must be controlled to prevent collapsing of adjacent structures. Various trenches and MEMS devices have been studied to produce very high aspect ratios with vertical profiles. Fig.7 and 8 show SEM pictures of very high etch aspect ratio of > 90:1 with minimal undercut.

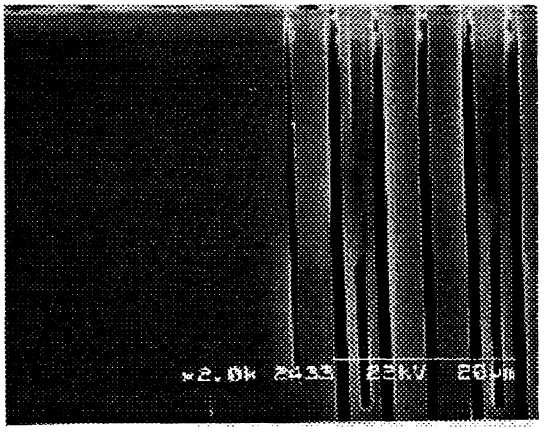

Fig.7 SEM picture of a high aspect ratio (90:1), Wafer size: 6".

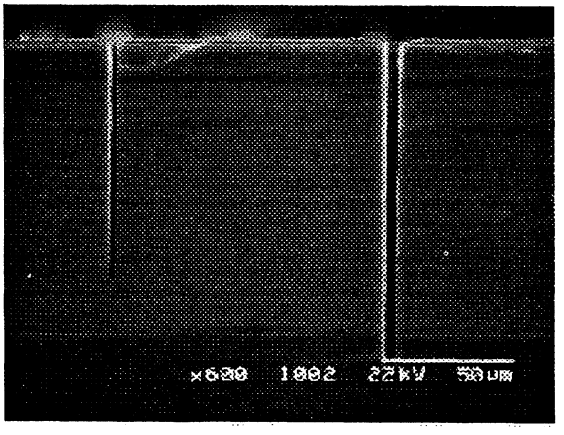

Fig.8 SEM pictures of a high aspect ratio (50:1), wafer size: 6".

6. HIGH SELECTIVITY TO MASK MATERIALS AND PROFILE CONTROL

The high selectivity to mask material becomes a necessity for MEMS applications on very deep or through wafer etching. The typical mask materials used are thermal silicon dioxide and photoresist. Other silicon dioxide by chemical vapor deposition (CVD) or low pressure chemical vapor deposition (LPCVD) can also be used as masks, but selectivity to these types of silicon dioxide is much lower than thermal silicon

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dioxide. If the selectivity is not sufficient during etching, it will require a thicker mask material. This will reduce the productivity and increases the over all cost of the wafer. To obtain a high selectivity to mask materials it is a balancing process between chemical and physical etch mechanisms. The selectivity decreases as physical etch increases, but if it is purely chemical then the device suffers from lost profile control and undercut. This is a delicate balance of all the combinations of process chemistry and reactor design.. Fig.9 and 10 show SEM pictures of very high selectivity to thermal silicon dioxide and photoresist mask. Surface charging can indeed develop an imbalance of electrons and ions. Negative profiles have been observed when silicon etching in high density plasma [3].

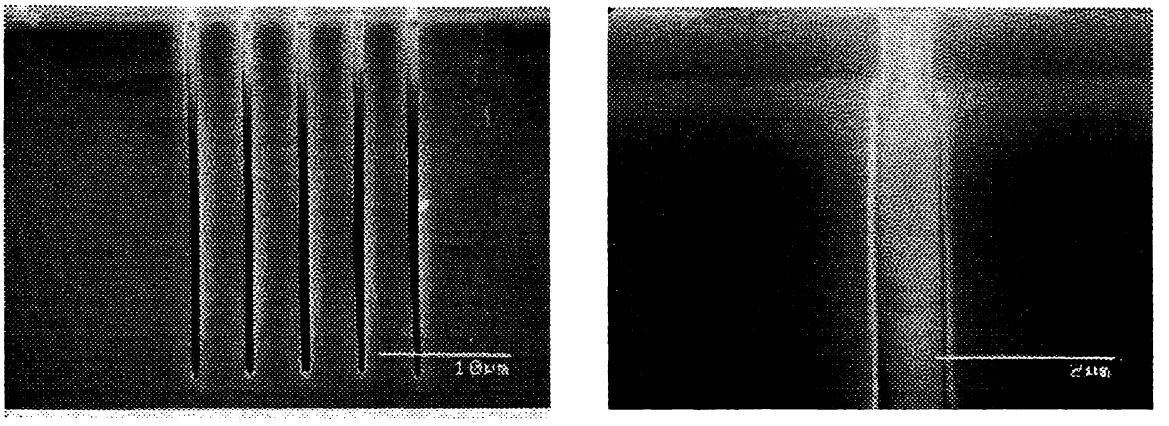

Fig. 9 SEM picture of high selectivity to thermal oxide mask >500:1

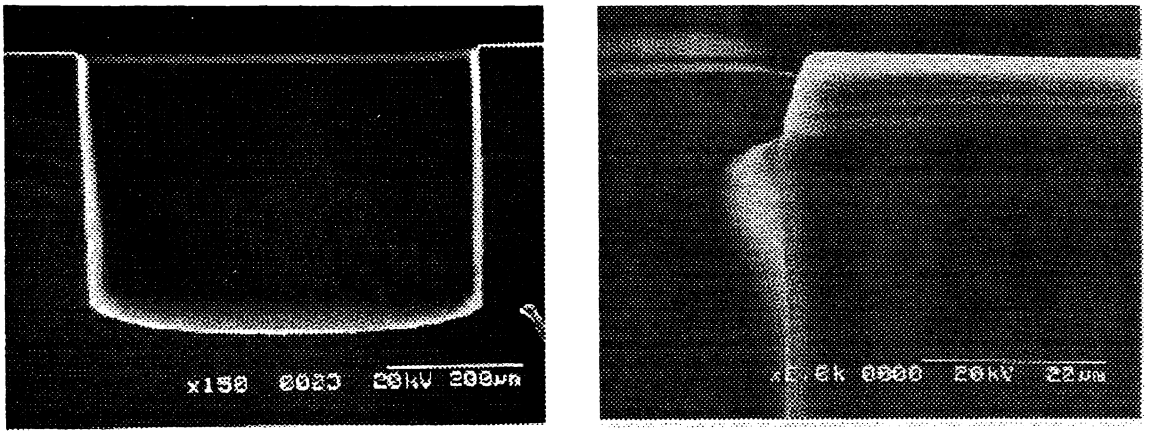

Fig. 10 SEM pictures of high selectivity to photoresist 250:1

A number of parameters can affect the mask selectivity materials such as substrate bias, pressure, power and etc. Pressure has a strong influence on selectivity. Selectivity increases as a function of pressure. Fig.11 shows the selectivity versus pressure on a thermal oxide mask.

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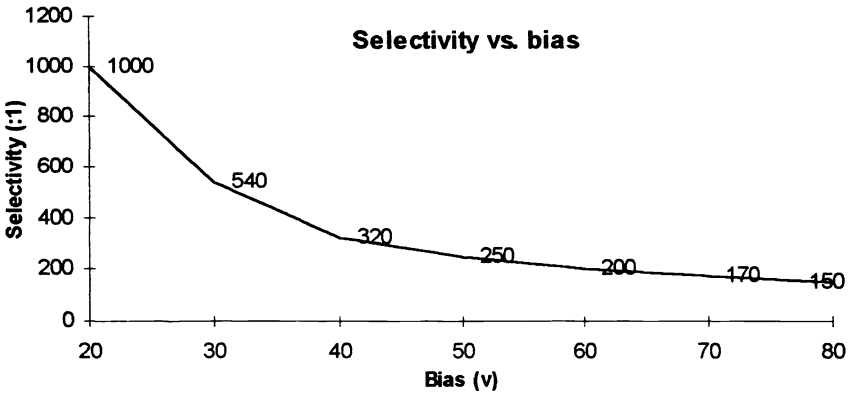

Fig. 11 shows pressure versus selectivity to a thermal oxide mask

7. ETCH DEPTH AND PROFILE UNIFORMITY

The etching uniformity on same feature sizes and profile control is important for wafer yield and consistent device performance. To minimize these two parameters, some other process parameter trade offs are needed such as etch rate, selectivity etc. Fig. 12 and 13 show SEM pictures of center and edge of a wafer on etch depth uniformity and profile control. The uniformity on same feature sizes is > $\pm$ 5.0% and vertical profile control on feature sizes range from 1.5μm to 20 μm.

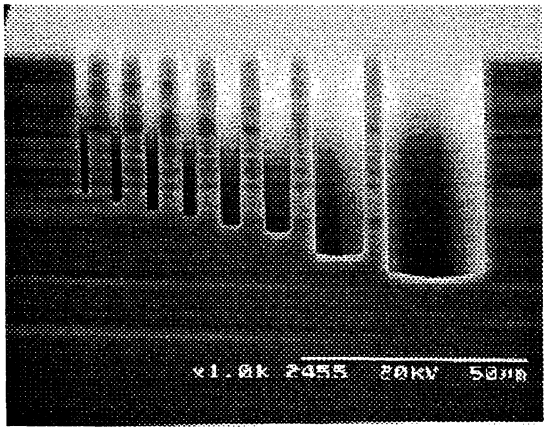

Fig. 12 shows etch depth uniformity and vertical profile control located on center of wafer

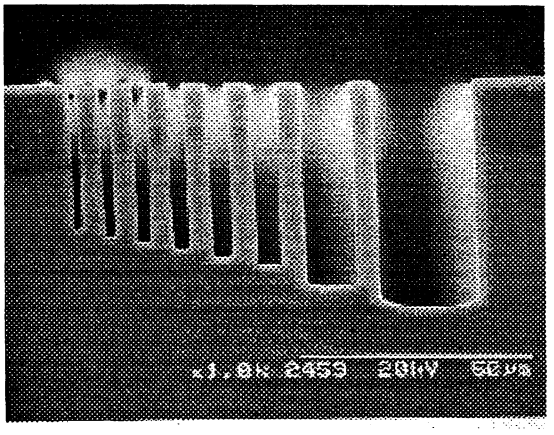

Fig. 13 shows etch depth uniformity and vertical profile control located near the edge of wafer

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8. CONCLUSION

MEMS applications (medical, automotive, electronic, etc.) will require advanced CMOS devices that combine electrical and mechanical functions. As device complexity increases, manufacturers are looking for low cost production techniques. Therefore, they will require that new equipment not only be production ready but also have a proven process that is production ready.

9. ACKNOWLEDGMENTS

The authors would like to express an appreciation to all those who provided device wafers for characterizing Alcatel's deep etching system. Some SEM pictures presented in this paper were obtained from these wafers.

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